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044_DEBUG_LPC
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047_USB3.1 TYPE-C+PI3DPX1205AZL
048_HDMI_DP159RSBT
049_ANT
050_Thermal Sensor & Fan
051_HDD_+++
052_USB3.1 Gen1*2 port
053_NGFF Type_WLAN&BT
054_OTHERS_+++
055_USB_+++
056_LED & CON
057_DSG_Discharge
058_Power Protect
059_EMI&Shield case
060_DC & BAT IN
061_OTHERS_+++
062_NFC_+++
063_NFC_+++
064_NFC_+++
065_ME_Hole & NUT
066_IO1_BOARD_PwrKeyBoard
067_OTHERS_+++
068_OTHERS_+++
069_OTHERS_+++
070_GFU_PCIE I/F
071_GFU_POWER
072_GFU_FRAME BUFFER
073_VRAM_Channel_A
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080_PW_TIGERLAKE (1) (6+2)
081_PW_TIGERLAKE (2) (6+2)
083_PW_+1.05VSUS_VNNEXT
084_PW_+1.8VSUS
086_PW_+1.2V/+VTT/+2.5V
087_PW_+3VADSW/+5VSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD (1) (N18E 7Phase)
092_PW_+NVVDD (2) (N18E 7Phase)
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094_PW_+FBVDDQ(N18)
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Tigerlake H Platform

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TGL PCH-H
HM570

32.768KHz
38.4MHz

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ASUSTeK COMPUTER INC.

Project Name	GX703_GU603
Rev	0.2
Title :	Block Diagram
Size	Custom
Dept.	Engineer:
Date	Wednesday, March 17, 2021
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ASUS	Project Name: GX502GX	Rev: R1.2
Title : CPU XDP		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 7 of 103	

CFG

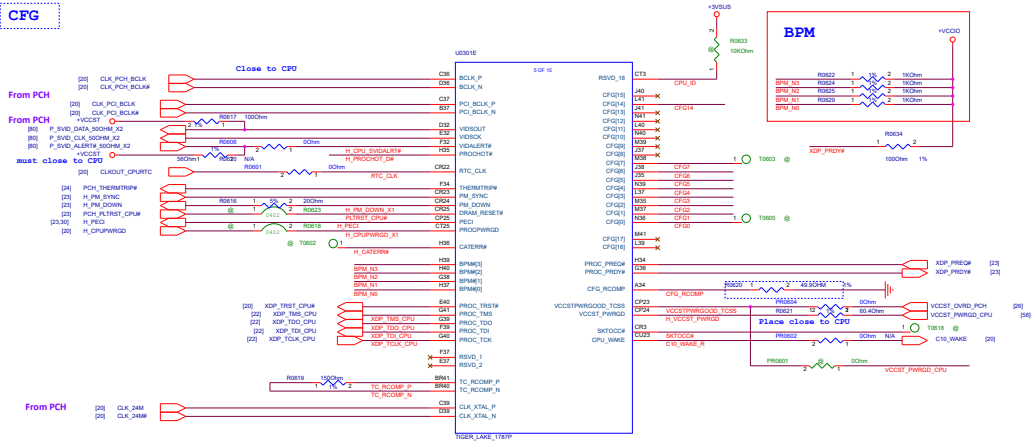
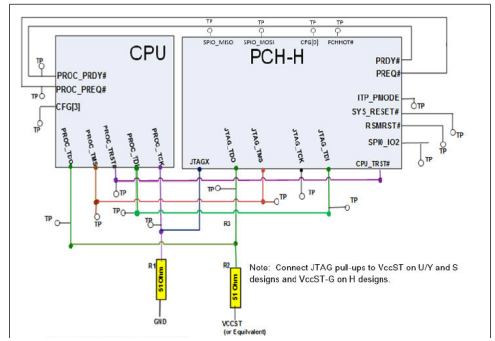
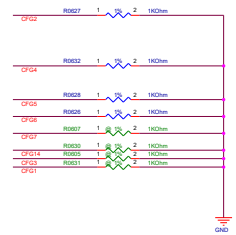


Figure 415. Connector Less Routing Topology



CFG Straps



Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

CFG Straps for Processor

ref : 575683-tgl-eds-vol1-rev0p97

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted
- Reserved Configuration Lane

CFG[1] : Reserved Configuration Lane
- Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal
- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed <====

CFG[3] : Reserved configuration lanes
- Reserved Configuration Lane

CFG[4] : eDP Enable
- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express* Bifurcation
- 00 : 1 x8 , 2 x4 PCI Express* <===
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

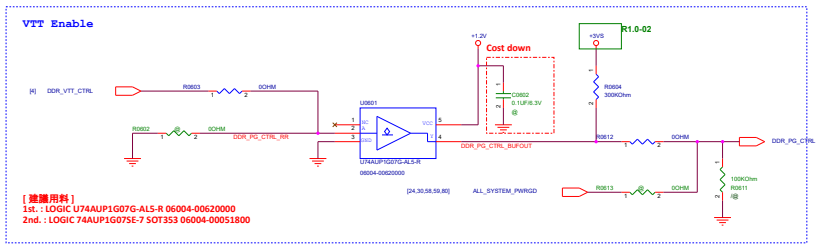
CFG[7] : PEG Training
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[13:8] : Reserved configuration lanes
- Reserved Configuration Lane

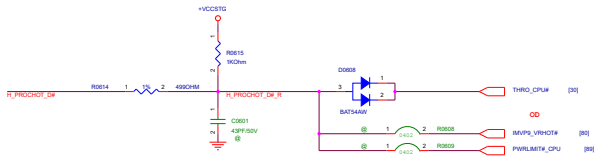
CFG[14] : PEG60 (PCIE4) Lane Reversal
- 1 : (Default) Normal <===
- 0 : Reversed

CFG[17:15] : Reserved configuration lanes
- Reserved Configuration Lane

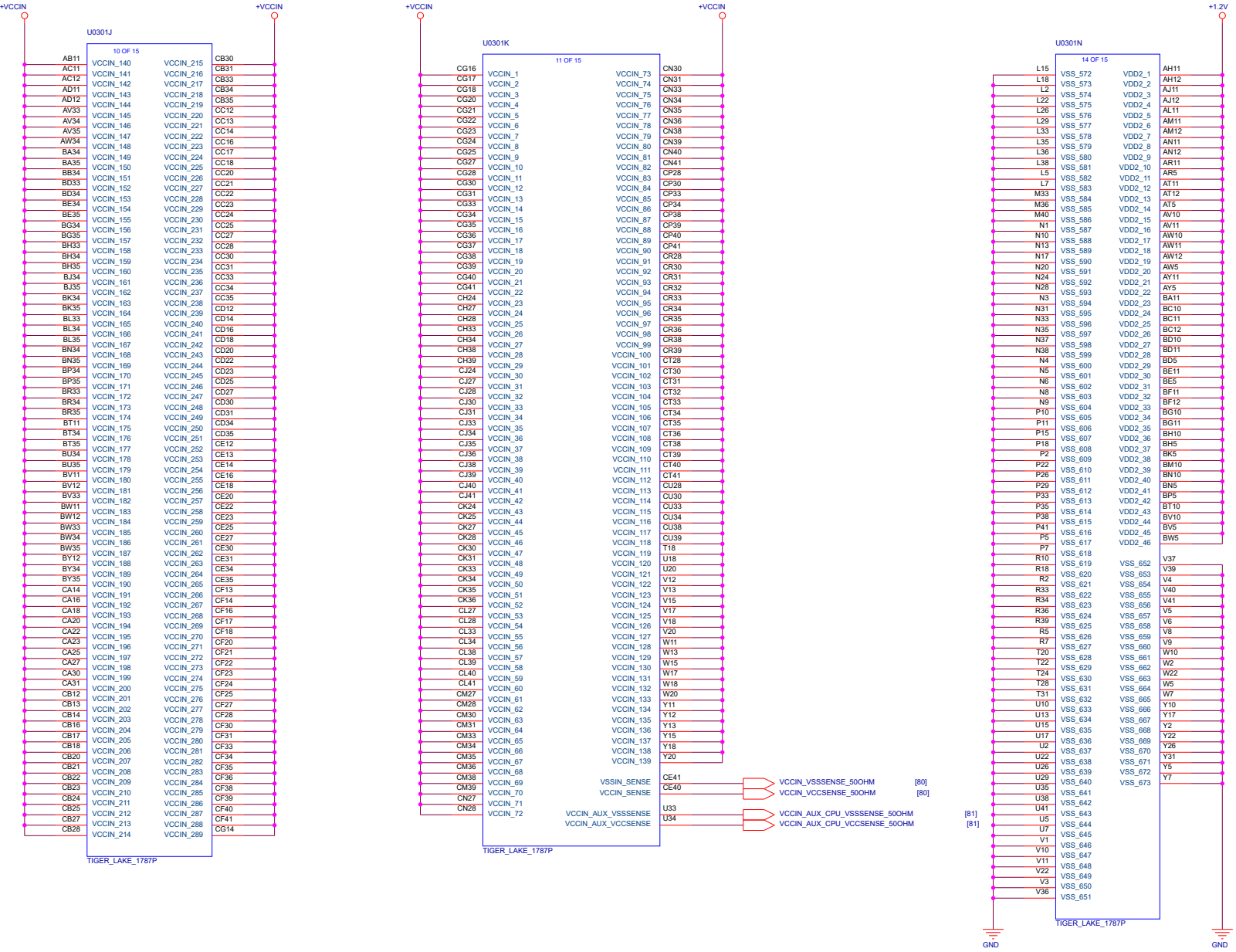
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116



CPU SIDEBAND SIGNALS



Project Name: GX502GX			Rev: R1.2
Title : CPU_CFG,RSVD			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 6 of 103		



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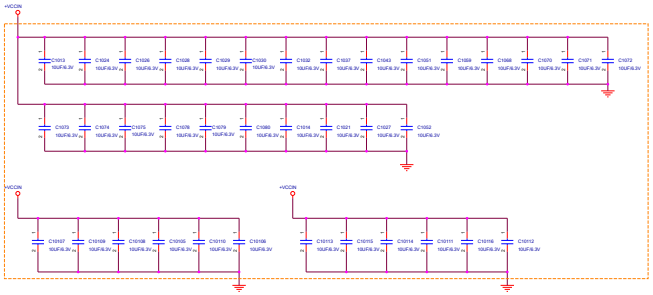
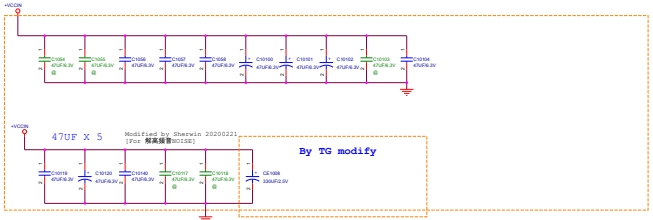
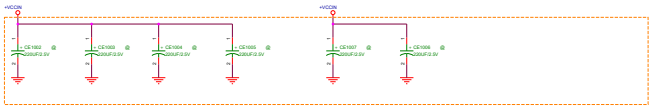
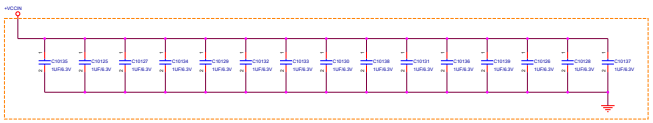
Project Name: GX502GX			Rev: R1.2
Title : CPU_PWR			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 9 of 103		

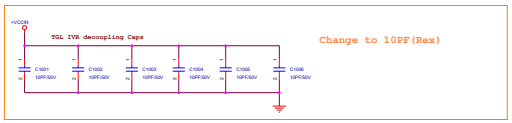
+VCCIN DECAPS

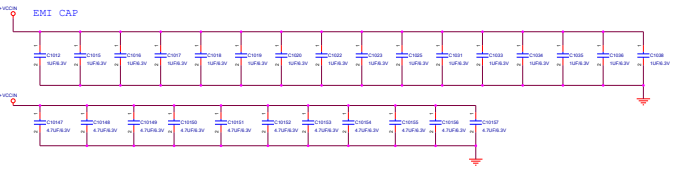








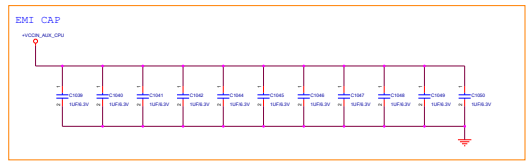


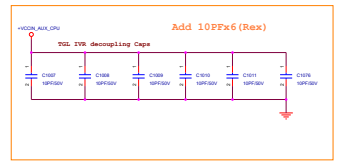


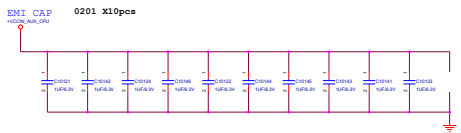
Decoupling Solution					
Power Rail	Decap Placement	Form Factor	Value	Number	Note
RVP REV1p0	VCCIN	Primary Side	7343		
			7343	220uF	6
		Secondary Side	0603	47uF	15
			0603	22uF	8
			0402	10uF	44
			0402		

Decoupling Solution					
Power Rail	Decap Placement	Form Factor	Value	Number	Note
BEP REV0p7	VCCIN	Primary Side	7343	330uF	4
			7343		
		Secondary Side	0603	47uF	12
			0603		
			0402	10uF	27
			0402		

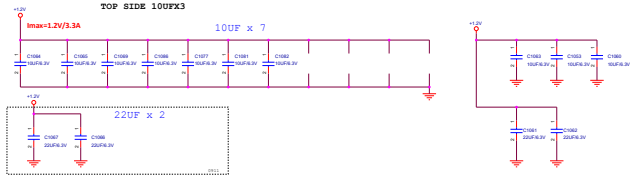
Decoupling Solution					
Power Rail	Decap Placement	Form Factor	Value	Number	Note
目前線路	VCCIN	Primary Side	7343	470uF	4 3上件1不上件
			3528	220F	6 均預留不上件
		Secondary Side	0603	47uF	15
			0603	22uF	24 均預留不上件
			0402	10uF	37
			0402		







+VDDQ DECAPS BACK SIDE 10UFX4/22UFX2
TOP SIDE 10UFX3



ASUS	Project Name: GX502GX		Rev: R1.2
Title:	010_CPU_POWER_CAP		
Size: B	Dept: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 10 of 103		

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	ESPI_IO0	Native	ESPI_IO0_PCH			
GPP_A1	ESPI_IO1	Native	ESPI_IO1_PCH			
GPP_A2	ESPI_IO2	Native	ESPI_IO2_PCH			
GPP_A3	ESPI_IO3	Native	ESPI_IO3_PCH			
GPP_A4	ESPI_CS#	Native	ESPI_CS#_PCH		PU 10K(@)	+3VSUS
GPP_A5	ESPI_CLK	Native	ESPI_CLK_PCH			
GPP_A6	ESPI_RST#	Native	ESPI_RST#_PCH			
GPP_A7	ESPI_CS1#	Native				
GPP_A8	ESPI_CS2#	Native				
GPP_A9	ESPI_CS3#	Native				
GPP_A10	ESPI_ALERT#	Native	ESPI_ALERT#_PCH		PU 10K(@)	+3VSUS
GPP_A11	NC	GPO				
GPP_A12	NC	GPO				
GPP_A13	NC	Native				
GPP_A14	NC	Native				

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	PCH_GPP_B0			
GPP_B1	GPO	GPO	PCH_GPP_B1			
GPP_B2	GPO	GPO	PCH_GPP_B2			
GPP_B3	GPO	GPO				
GPP_B4	NC					
GPP_B5	SRCCLKREQ0#	Native	CLK_PEGA_REQ0# _R1		PU10K(@) /3V10K	+3VSUS
GPP_B6	NC					
GPP_B7	SRCCLKREQ1#	Native	CLK_REQ1#/CLKREQ2_WLAN#		PU 10K	+3VSUS
GPP_B8	NC					
GPP_B9	NC					
GPP_B10	SRCCLKREQ5#	Native	CLK_REQ5#/CLKREQ5_NGFF1#		PU 10K	+3VSUS
GPP_B11	NC					
GPP_B12	SLP_S0#	Native	SLP_S0# (TP)			
GPP_B13	PLTRST#	Native	PLT_RST#		PU 100K	
GPP_B14	GPO	Strap	PCH_GPP914		PU10K(@) /3V10K(@)	+3VS
GPP_B15	GPO	GPO	WLAN_ON#		PU 10K(@)	+3V_WLAN
GPP_B16	NC					
GPP_B17	NC					
GPP_B18	GPO	Strap	PCH_GPP918		PU10K(@) /3V10K(@)	+3VS
GPP_B19	GPO	GPO	WT_ON_PCH		PU10K(@) /3V10K(@)	+3V_WIFI_MAIN
GPP_B20	NC					
GPP_B21	GPI	GPI	PCH_GPP921/WV_GC6_FB_EN		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPP922		PU10K(@) /3V10K(@)	+3VS
GPP_B23	GPO	GPO	PCH_GPP923		PU 150K(@)	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	SPI	Strap	GPP_C2_WT_GAST_MASK_N		PU 4.7K	+3VSUS
GPP_C3	NC					
GPP_C4	NC					
GPP_C5	GPO	Strap	PCH_GPPC5	PD	PU10K(@) /3V10K 5%(@)	+3VSUS
GPP_C6	NC					
GPP_C7	NC					
GPP_C8	SPI	GPO	PCH_GPPC8/SGPU_PWROK		PD 10K(@)	
GPP_C9	GPO	GPO	PCH_GPPC9/GPU_EN2#		PD 10K(@)	
GPP_C10	NC					
GPP_C11	GPI	GPI	CPAD_INT#		PU 10K	+3VS
GPP_C12	GPI	GPI	DIMM_SEL0		PU10K(@) /3V10K(@)	+3VSUS
GPP_C13	GPI	GPI	DIMM_SEL1		PU10K(@) /3V10K(@)	+3VSUS
GPP_C14	GPI	GPI	DIMM_SEL2		PU10K(@) /3V10K(@)	+3VSUS
GPP_C15	GPI	GPI	NFC_ID		PU10K(@) /3V10K	+3VSUS
GPP_C16	I2C0_SDA	Native	I2C1_SDA			
GPP_C17	I2C0_SCL	Native	I2C1_SCL			
GPP_C18	I2C1_SCL	Native	I2C1_SDA		PU 1K	+3VS
GPP_C19	I2C1_SCL	Native	I2C1_SCL		PU 1K	+3VS
GPP_C20	UART2_RXD	Native	UART2_RXD		PU 51K	+3VS
GPP_C21	UART2_TXD	Native	UART2_TXD		PU 51K	+3VS
GPP_C22	UART2_RTS#	Native	UART2_RTS#		PU 51K	+3VS
GPP_C23	UART2_CTS#	Native	UART2_CTS#		PU 51K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	PCB_ID1		PU10K(@) /3V10K(@)	+1.8VSUS
GPP_D1	GPI	GPI	PCB ID0		PU10K(@) /3V10K(@)	+1.8VSUS
GPP_D2	NC					
GPP_D3	NC					
GPP_D4	NC	Native	SMB_SCL_PCH		PU 2.2K	+1.8VSUS
GPP_D5	I2S2_SFRM	Native	PCH_GPP05 / M.2_BT_PCMFRM_CAP_SEL_R		PU 75K	
GPP_D6	I2S2_TXD	Native	PCH_GPP06 / M.2_BT_PCMOUT_CAP(@)		PU 75.5K	
GPP_D7	I2S2_RXD	Native	PCH_GPP07 / M.2_BT_PCMCLK			
GPP_D8	I2S2_SCLK	Native	PCH_GPP08 / M.2_BT_PCMCLK			
GPP_D9	SMLOCLK	Native	SMCLK CLK		PU 2.2K	+1.8VSUS
GPP_D10	SMLODATA	Native	SMCL DAT		PU 2.2K	+1.8VSUS
GPP_D11	NC					
GPP_D12	NC					
GPP_D13	NC					
GPP_D14	NC					
GPP_D15	SML1DATA	Native	SMC_SDA_PCH		PU 2.2K	+1.8VSUS
GPP_D16	NC					
GPP_D17	NC					
GPP_D18	NC					
GPP_D19	NC					
GPP_D20	NC					
GPP_D21	NC					
GPP_D22	NC					
GPP_D23	NC					

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	NC					
GPP_E1	GPI	Native	SSD_DET1		PU 10K	+3VS
GPP_E2	NC					
GPP_E3	GPI	GPI	SNI#		PU 10K	+3VS
GPP_E4	NC					
GPP_E5	GPO	GPO	BGPP1_SEVSLP		PD 10K(@)	+3VS
GPP_E6	NC					
GPP_E7	GPI	GPI	XCI#		PU 10K	+3VS
GPP_E8	NC					
GPP_E9	GPI	Native	USB_OC#0		PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	BM_BATLOW#		PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 1K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUS3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUS4#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#		Test Point	
GPD7	GPO7	Strap	TEST_MIX_ADT#		PD 20K	
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		Test Point	
GPD10	SLP_S5#	Native	SLP_S5#		PD 100K(@)	
GPD11	NC					
GPD12	NC					

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_S0	NC					
GPP_S1	NC					
GPP_S2	NC					
GPP_S3	NC					
GPP_S4	NC				Test Point	
GPP_S5	NC				Test Point	
GPP_S6	NC				Test Point	
GPP_S7	NC				Test Point	

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	NC					
GPP_F1	NC					
GPP_F2	NC					
GPP_F3	NC					
GPP_F4	GPO	GPO	BB_FORCE_PWR_PCH		PD 10K	
GPP_F5	NC					
GPP_F6	NC					
GPP_F7	NC					
GPP_F8	NC					
GPP_F9	NC					
GPP_F10	NC					
GPP_F11	NC					
GPP_F12	NC					
GPP_F13	NC					
GPP_F14	NC					
GPP_F15	NC					
GPP_F16	NC					
GPP_F17	NC					
GPP_F18	NC					
GPP_F19	GPO	Native	X_VIDEN_PCH		PU 100K	
GPP_F20	GPO	Native	LCD_BACKEN_PCH		PU 100K	+3VSUS
GPP_F21	GPO	Native	X_BKLTCTL_PCH		PU10K(@) /3V10K(@)	+3VS_LCD
GPP_F22	GPO	Native	VNN_CTRL_PCH			
GPP_F23	NC					

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	NC					
GPP_G1	NC					
GPP_G2	SMB_FORCE_RELOAD	Native	SMB_FORCE_RELOAD			
GPP_G3	NC					
GPP_G4	NC					
GPP_G5	NC					
GPP_G6	NC					
GPP_G7	NC					
GPP_G8	NC					
GPP_G9	NC					
GPP_G10	NC					
GPP_G11	NC					
GPP_G12	SGPU_CTRLCLK_LS00	Native	SGPU_CTRLCLK_LS00		PU10K(@)	
GPP_G13	SGPU_CTRLDATA_TEST_LS00	Native	SGPU_CTRLDATA_TEST_LS00		PU10K(@)	
		Strap				
GPP_G14						
GPP_G15						

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	NC					
GPP_H1	GPI	Native	CLKREQ7_NGFF2#		PU 10K	+3VS
GPP_H2	GPI	Native	CLKREQ8_GLAN#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLKREQ9_CR#		PU 10K	+3VS_CR_AUX
GPP_H4	NC					
GPP_H5	NC					
GPP_H6	NC					
GPP_H7	NC					
GPP_H8	NC					
GPP_H9	NC					
GPP_H10	NC					
GPP_H11	NC					
GPP_H12	GPI	Strap	GPP_H12		PD 20K(@)	
GPP_H13	NC					
GPP_H14	NC					
GPP_H15	GPI	GPI	SML3ALERT#		PU10K(@) /3V10K 5%	+3VSUS
GPP_H16	NC					
GPP_H17	NC					
GPP_H18	GPI	GPI	SML4ALERT#		PU10K(@) /3V10K	+3VSUS
GPP_H19	GPI	GPI	ALT_GP_WP0#		PU 10K	+3VS
GPP_H20	NC					
GPP_H21	NC					
GPP_H22	NC					
GPP_H23	NC					

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	SML_IRQ_PCH		PU 10K	+3VSUS
GPP_I1	GPI	Native	Test Point			
GPP_I2	NC					
GPP_I3	NC					
GPP_I4	NC					
GPP_I5	SDC_CLK	Native	SDIB_WDAT/SDC_CLK		PU 10K	+3VS
GPP_I6	SDC_DATA	Native	SDIB_WDAT/SDC_DATA		PU 10K	+3VS
GPP_I7	NC					
GPP_I8	GPO	GPO	GPP_I8_CR_RST		PU 5.1K(@)	+3VS_CR
GPP_I9	GPO	GPO	GPP_I9_SO_PWREN		PU 100K	
GPP_I10	GPI	GPI	GPP_I10_CR_WAKE#		PU 10K	+3VS_CR_AUX
GPP_I11	GPI	GPI	USB_OC#4		PU 10K	+3VSUS
GPP_I12	GPI	GPI	USB_OC#5		PU 10K	+3VSUS
GPP_I13	GPI	GPI	USB_OC#6		PU 10K	+3VSUS
GPP_I14	GPI	GPI	USB_OC#7		PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	NC					
GPP_J1	GPO	GPO	CPU_C10_GATE#_PCH		PD 75K/PD 330K(@)	+1.8VSUS
GPP_J2	CNV_RGI_DT	Native	CNV_RGI_DT_PCH		PU 10K(@) /PD 10K	+1.8VSUS
GPP_J3	CNV_RGI_RSP	Native	CNV_RGI_RSP			
GPP_J4	CNV_RGI_DT	Native	CNV_RGI_DT_PCH		PU 20K	+1.8VSUS
GPP_J5	CNV_RGI_RSP	Native	CNV_RGI_RSP			
GPP_J6	CNV_MFUART2_RXD	Native	CNV_MFUART2_RXD			
GPP_J7	CNV_MFUART2_TXD	Native	CNV_MFUART2_TXD			
GPP_J8	NC					
GPP_J9	NC					

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	NC					
GPP_K1	GPI	GPI	KBID_0		PU 10K(@) /PD 10K(@)	+3VSUS
GPP_K2	GPI	GPI	KBID_1		PU 10K(@) /PD 10K(@)	+3VSUS
GPP_K3	GPI	GPI	KBID_2		PU 10K(@) /PD 10K(@)	+3VSUS
GPP_K4	GPO	GPO	HDA_SWITCH			
GPP_K5	GPO	GPO	DDPB_PWR_EN#		PU 100K	+3VS
GPP_K6	TBT	Native	ESPI_HPD_CPU		PD 100K	
GPP_K7	DDIB_HDMI_HPD	Native	DDIB_HDMI_HPD		PU 10K(@)	+3VS
GPP_K8	CORE_VID0	Native	VCCIN_AUX_CORE_VID0		PU 100K	+3VSUS
GPP_K9	CORE_VID1	Native	VCCIN_AUX_CORE_VID1		PU 100K	+3VSUS
GPP_K10	NC					
GPP_K11	NC					

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_R0	HDA_BCLK	Native	ACS_BCLK_AUD_X1			
GPP_R1	HDA_SYNC	Native	ACS_SYNC_AUD_X1			
GPP_R2	HDA_SDO	Native	ACS_SDOUT_AUD_X1		PU 3.2K	+3VSUS/PD_SPI_10K
GPP_R3	HDA_SDI0	Native	ACS_SDIN0_AUD			
GPP_R4	HDA_RST#	Native	ACS_RST#_AUD_X1			
GPP_R5	NC					
GPP_R6	NC					
GPP_R7	NC					
GPP_R8	NC					
GPP_R9	NC					
GPP_R10	NC					
GPP_R11	NC	Native	SX_EXIT_HOLDOFF_N			
GPP_R12	NC	Native	GPP_R12_CLKOUT48			
GPP_R13	NC					
GPP_R14	NC					
GPP_R15	NC					
GPP_R16	NC					
GPP_R17	NC					
GPP_R18	NC					
GPP_R19	GPO	GPO	ESP_ON#		PD 100K	

EC GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PU 1M	
GPA1	OD	GPO	CHG_LED#	PU 750	+5VSUS
GPA2	OD	GPO	CHG_FULL_LED#	PU 560	+5VSUS
GPA3	Alt	PWM	FAN1_PWM		
GPA4	Alt	PWM	NC		
GPA5	Alt	PWM	FAN2_PWM		
GPA6	O	GPO	FAN_V_Switch	PU 100K	+3VA
GPA7	O	GPO	EC_ESP_PWR		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_DC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 10K	+3VA
GPB2	OD	GPO	RSTP_PWR#	PU 10K	3.3V_S_5V_SYSON
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	HKey_MD2#	PU 10k	
GPB6	OD	GPO	AMP_SLEEP#	PU 100K	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	NC				
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	Alt	GPO	BOT_PCT_RST#	PU 100K	
GPC4	I	GPI	EC_GPC4/PM_SUS@#	PU 100K	
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU10K(@) /3V10K	+3VA_EC
GPC7	O	GPO	EC_GPC7/HDEV_PWR_EN	PU 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	CPU_C10_GATE#	PU 100K	+3VSUS
GPD1	O	GPO	EC_GPD1/SMI_AC_PRESENT		
GPD2	Alt	GPO	ESPI_RST#	PU 100K	
GPD3	O	GPO	SCI#	PU 10K	+3VS
GPD4	O	GPO	SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/CP_SI#	PU 10K	+3VS
GPD6	Alt	GPI	FAN2_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PU 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PU 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPE4	O	GPO	VGSI_ON	PU 100K&PD 1M	+3VA_EC
GPE5	O	GPI	3VAUDM_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	EC_GPE6		
GPE7	OD	GPO	TYBO_CTS#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	PM_PWRGT#@	PU 100K(@)	+3VSUS
GPF1	O	GPO	FP_RESET		
GPF2	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPF4	O	GPO	FP_SSO_EC	PU 1M	
GPF5	I	GPI	FP_AOC_EC	PU 100K	+3VA_EC
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	I	GPI	ADP_INSERT_WO#	PU 100K	+3VA
GPG2	I	Strap	EC_GPG2	PU 100K	+3VA_EC
GPG6					

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	NA	GPO			
GPH1	Alt	SMBus	P_SMB5_CLK	PU 2.2K	+3VA_EC
GPH2	Alt	SMBus	P_SMB5_DAT	PU 2.2K	+3VA_EC
GPH3	O	GPO	PM_S2AG2CF#	NC 10K(@) /PD 10K(@)	+3VSUS
GPH4	O	GPO	DPWROK_EC	PU 10K	
GPH5	O	GPO	PM_PWROK	PU 10K	
GPH6	O	GPO	PM_SYSPWROK@	PU 10K	
GPH7	O	GPO	LCD_BACKOFF#	PU 100K	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#	PU 100K	
GPI1	I	GPI	3VSUS_PWRGD	PU 100K	+3VA_DSW
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP9_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	Alt	ADC	MB_MAX_POWER	NC 560K/PD 100K	+3VACC
GPI6	Alt	ADC	A/D_MAX_POWER	PU 100K/PD 100K	+3VACC
GPI7	Alt	ADC	P_IADP_IO		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	I	GPI	TBT_PD1_PROCHOT#		
GPJ1	I	GPI	GC_STATE_EC		
GPJ2	I	GPI	PD1_I2C_INT_EC	PU 100K	+3VA_EC
GPJ3	O	GPO			
GPJ4	O	GPO	EC_OV_DDR	PU 100K	
GPJ5	O	GPO	ADAPTER_INM_R	PU 100K	+3VA_EC
GPJ6	I	GPI	HKey_INT#	PU 100K	+3VA_DSW_PWRGD
GPJ7	O	GPO	NVDD_PWR_SEL	PU 10K(@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EC00	EC00	ESPI_IO0		
GPM1	LAD1/EC01	EC01	ESPI_IO1		
GPM2	LAD2/EC02	EC02	ESPI_IO2		
GPM3	LAD3/EC03	EC03	ESPI_IO3		
GPM4	LPCCLK/ESCK	ESCK	ESPI_CLK		
GPM5	LFRAME#/ECS#	ECS#	ESPI_CS#	PU 10K(@)	+1.8VSUS
GPM6	SERIRQ/ALERT#	ALERT#	ESPI_ALERT#	PU 10K(@)	+1.8VSUS

GX703/GU603 Source:

SMLink/SM_BUS ADDRESS :

PCH Master (SMBUS)	
SM-Bus Device	**SM-Bus Address**
SO-DIMM	0xA4

PCH Master (SMLink0)	
SMLink Device	**SMLink address**

PCH Master (SMLink1)	
SMLink Device	**SMLink address**
PD	0x40

EC Master (SMB0)	
SM-Bus Device	**SM-Bus Address**
SN1060,RICHTA(CHARGER)	0x12
BATTERY(GAUGE)	0x16
AFL6012(PROTECTION)	0x7E

EC Master (SMB1)	
SM-Bus Device	**SM-Bus Address**
GPU Thermal sensor	0x98
CPU Thermal sensor	0x90
VRAM Thermal Sensor	0x92
ITE(SYS(N-key)	0xE2
VGA 3W Thermal sensor	

EC Master (SMB3)	
SM-Bus Device	**SM-Bus Address**
Slave charger	0x12
VCCIN_AUX_CPU Controller	0x21
VCCIN Controller	0x20
FD	0x42,0x4A
Smart Amplifier	0x98

USB2.0	GX70L Devices Assign	GU603L Devices Assign
USB2.0 #1		
USB2.0 #2		
USB2.0 #3	(Port1)USB3.2 Gen2 Type(C)(4701)	(Port1)USB3.2 Gen2 Type(C)(4701)
USB2.0 #4	(Port3)USB3.2 Gen2 Type(A)(3801)	(Port3)USB3.2 Gen2 Type(A)(3801)
USB2.0 #5		(Port2)USB3.2 Gen2 Type(A)(5202)
USB2.0 #6	FigerPrinter(CDP)(5601)	
USB2.0 #7		
USB2.0 #8	Thunderbolt(I)(3201)	Thunderbolt(I)(3201)
USB2.0 #9	FigerPrinter(CDP)(5635)	
USB2.0 #10	N-key(U5509)	N-key(U5509)
USB2.0 #11	(Port2)USB3.2 Gen2 TypeA(4701)	
USB2.0 #12	(Port3)USB3.2 Gen2 TypeA(4702)	
USB2.0 #13	N-key(U3506)	
USB2.0 #14	BTU(U501)	BTU(U501)

Project Name	GX703_GU603	Rev 0.2
Title :	System Setting	
Size:	Document Number:	
Date:	Sheet of	
Dept.:	Engineer:	

<Core Design>

Title : DDR4_ON-BOARD_A2

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.2

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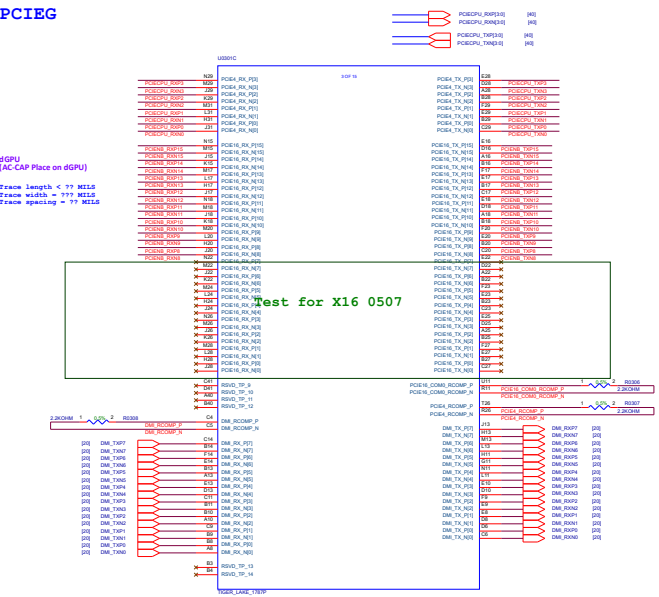

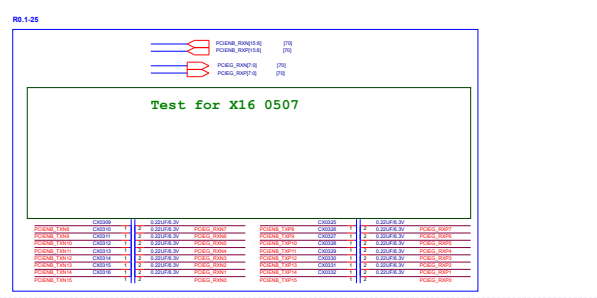

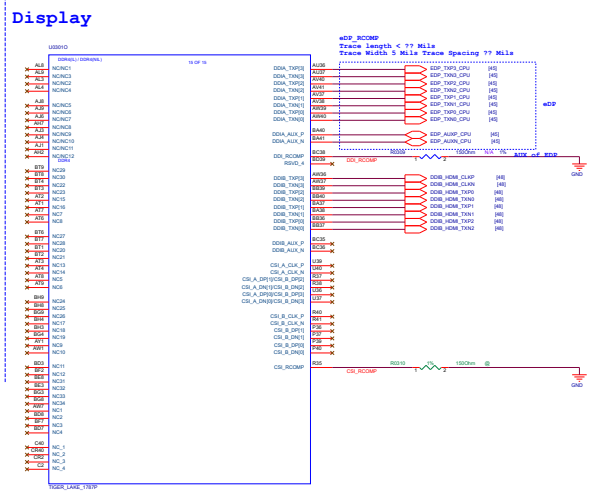

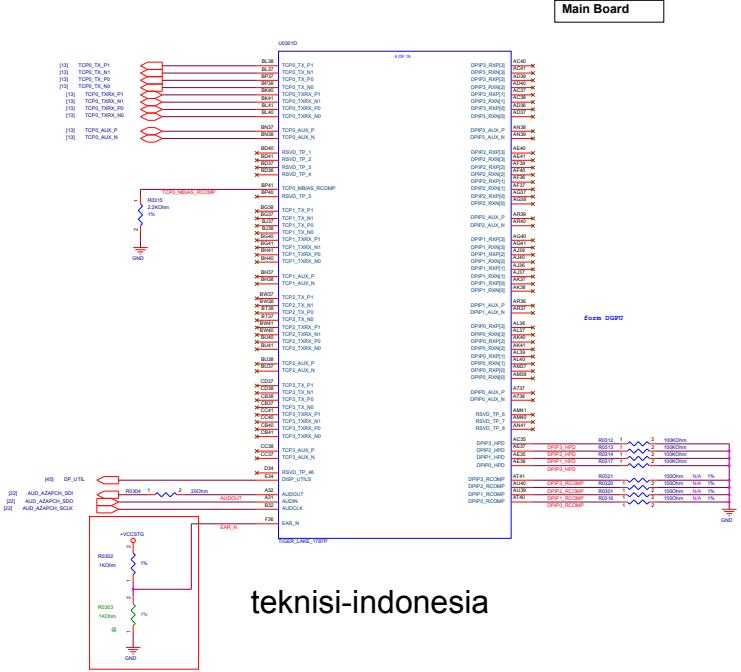

Table 81. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes: 1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.

2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.
   - For example:
     a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
     b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
     c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Disabling and Termination Guidelines for the Intel High Definition Audio Interface and the Intel Display Audio Interface

When the Intel HD Audio interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI on the CPU need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO on the CPU can be left unconnected. The Intel Display Audio pins on the PCH may be left unconnected.

ASUS Project Name GX502GX Rev 81.2
Title : CPU_DMI,PEG,FDI,eDP,DDI
Size Custom Dept.: ASUSTeK COMPUTER Engineer: EE
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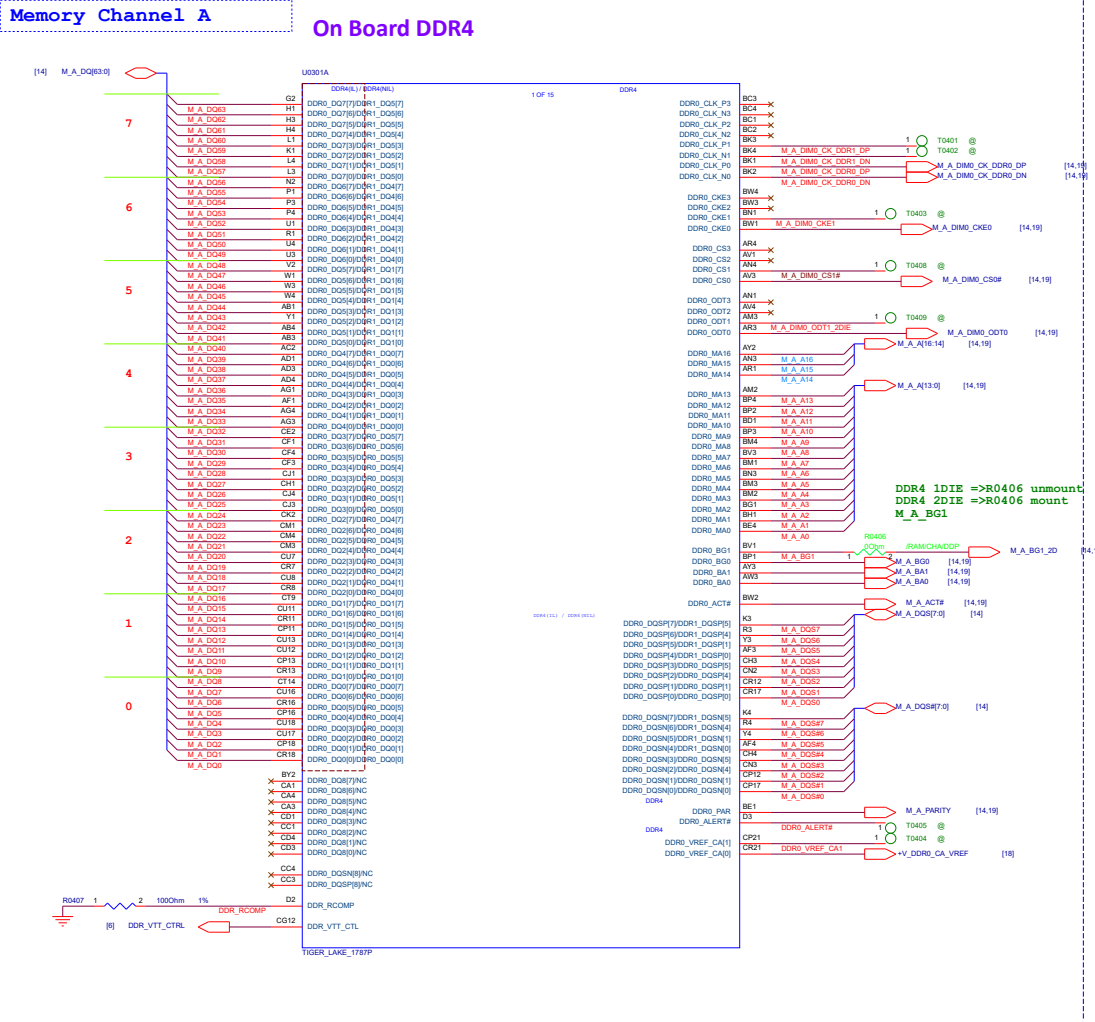
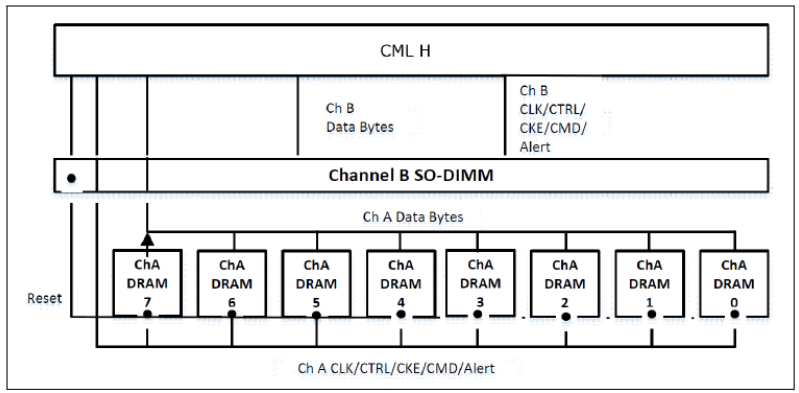


Figure 72. CML H DDR4 x8 Memory Down Placement and Block Diagram



Config # / Chapter	Tech	Topology	Frequency	Memory Device	Device Ballout	PCB Stackup	IL/NIL
TGL H DDR4 Mixed SODIMM and Memory Down x8 Daisy Chain Topology on page 85	DDR4	Mixed SODIMM and MD x8 Daisy-Chain (8 DRAM per channel)	3200	**SODIMM:** RC-A(1Rx8) RC-E(2Rx8) RC-C(1Rx16) **Memory Down:** SDP x8	SODIMM :260 MDx16: 78	Type3-10L	IL

ASUS	Project Name: GX502GX				Rev: R1.2
Title : CPU_DDR4					
Size: C	Dept.: ASUSTeK COMPUTER		Engineer: EE		
Date: Wednesday, March 17, 2021	Sheet 4 of 103				

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Title : NB_****

ASUSTeK COMPUTER

Engineer: EE

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A	GX502GX	R1.2

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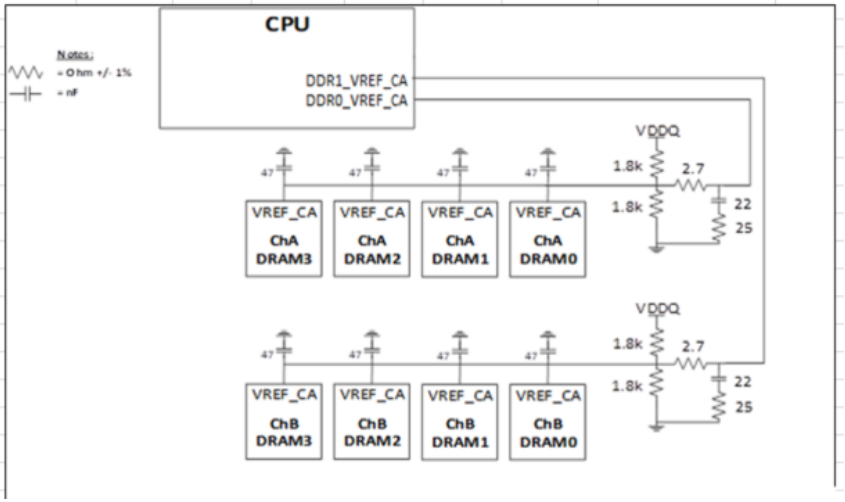
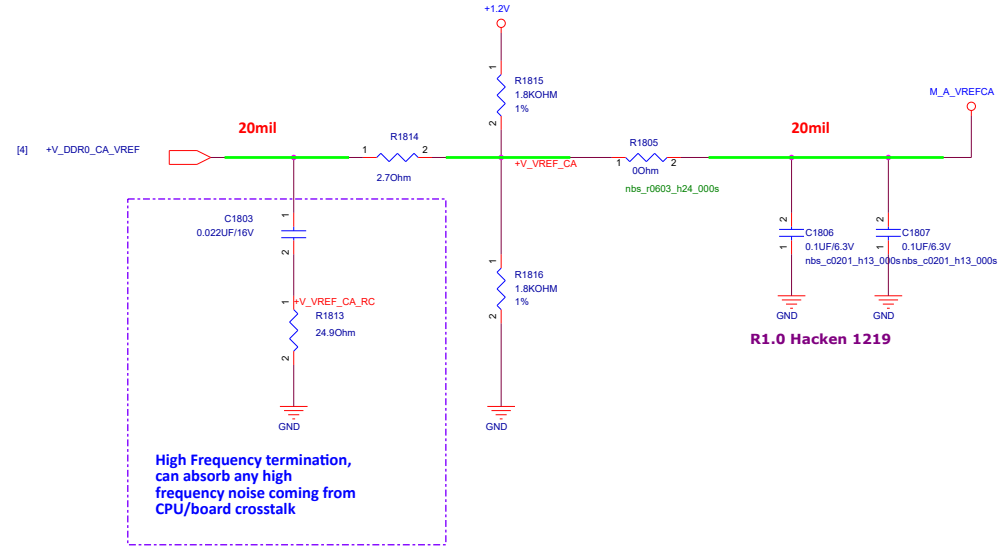
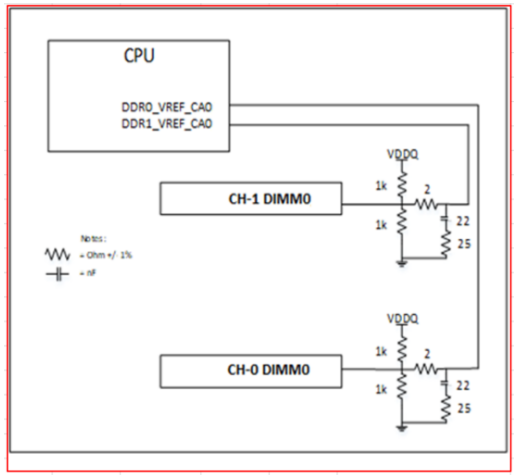
Main Board

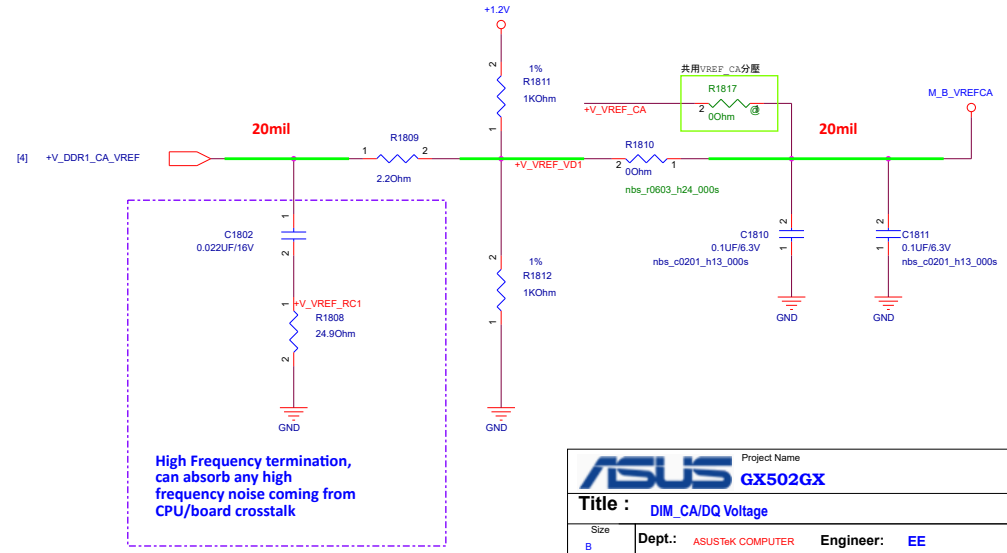
Memory Down Vref





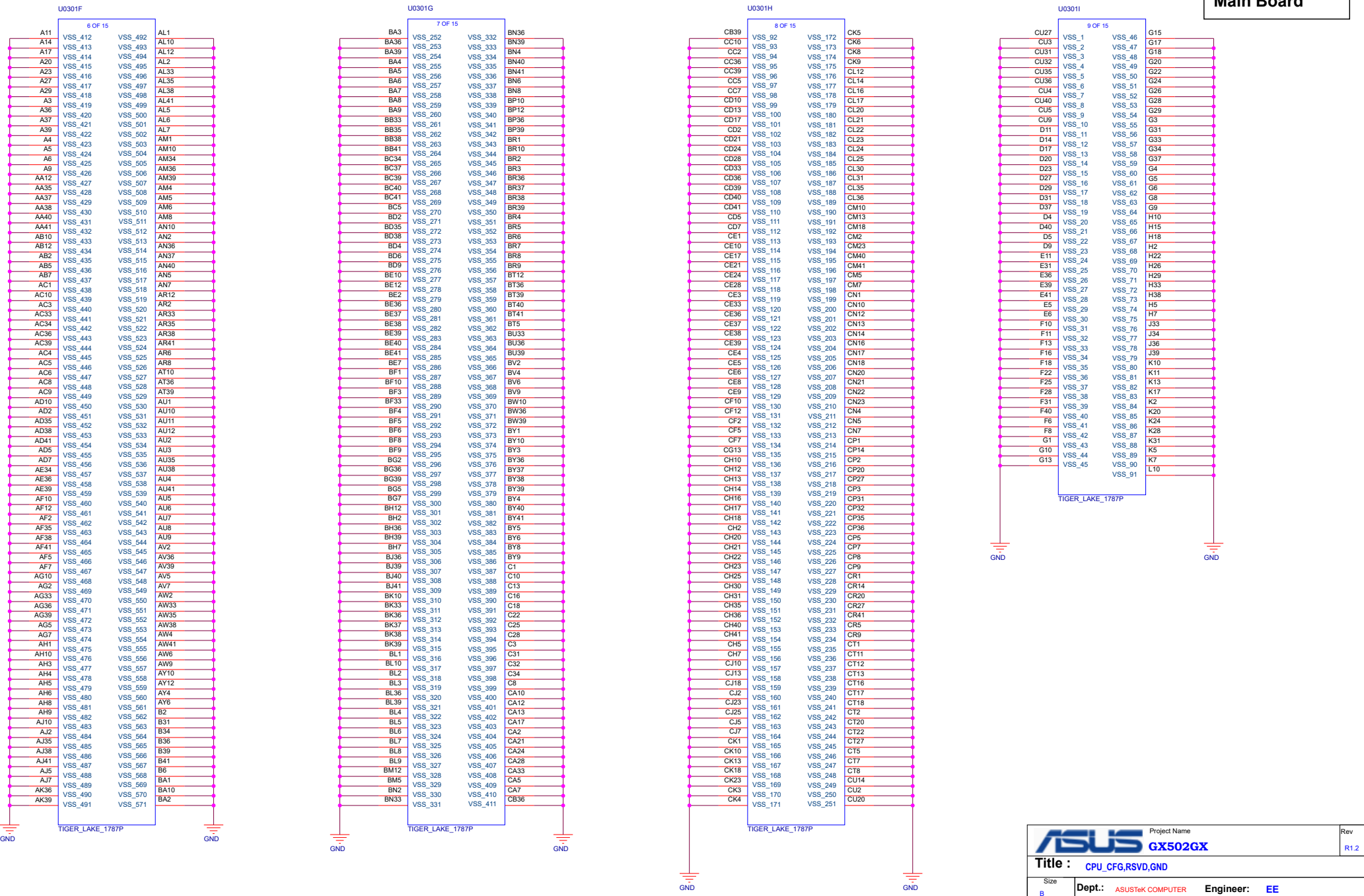
SO-DIMM1 Vref



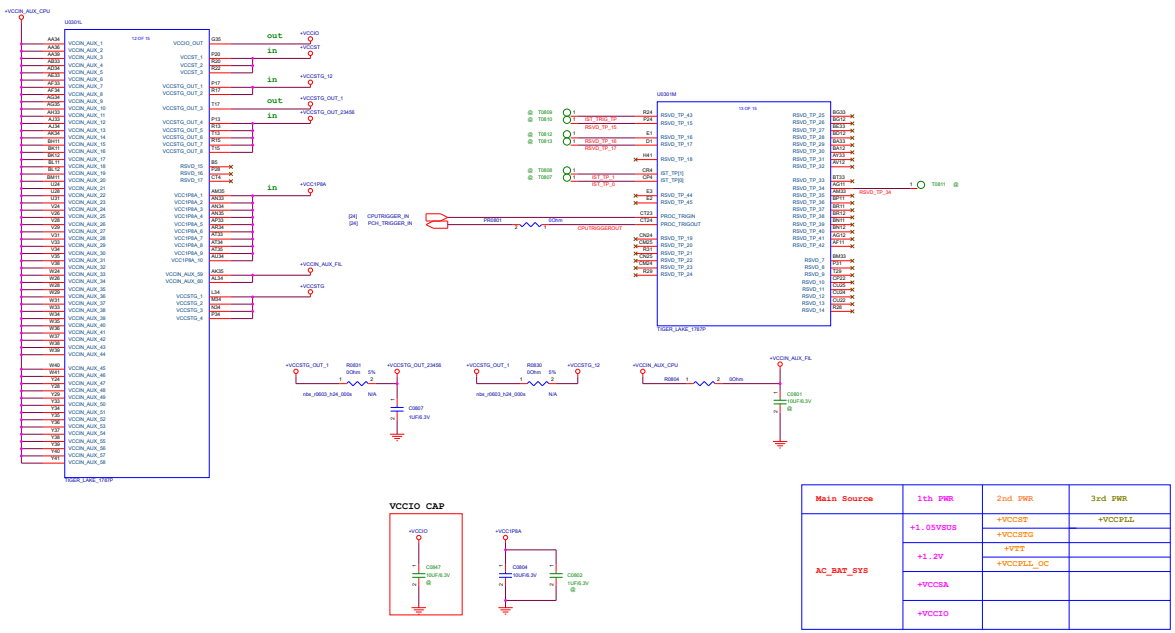


ASUS	Project Name: GX502GX	Rev: R1.2
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 18 of 103	

Main Board

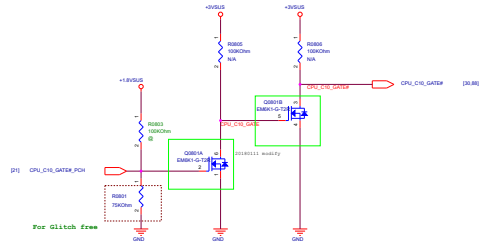


ASUS	Project Name: GX502GX	Rev: R1.2
Title :	CPU_CFG,RSVD,GND	
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 5 of 103	



Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	+VCCPLL
		+VCCSTG	
	+1.2V	+VTT	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO		

Main Board

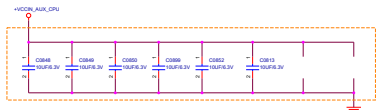


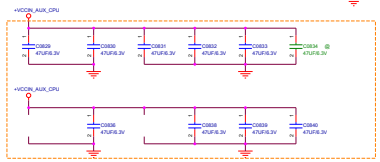
Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+3$~30mW
VccPLL_OC off in S0ix/C10	On in S0ix/C10	+3~10mW
VccPLL_OC off in S0ix	On in S0ix	+3~10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off Vcc5TG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

+VCCIN_AUX_CPU DECAPS





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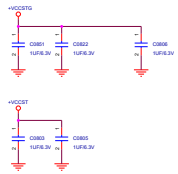
+VCCST & +VCCSTG DECAPS Place Back Side (TOP)

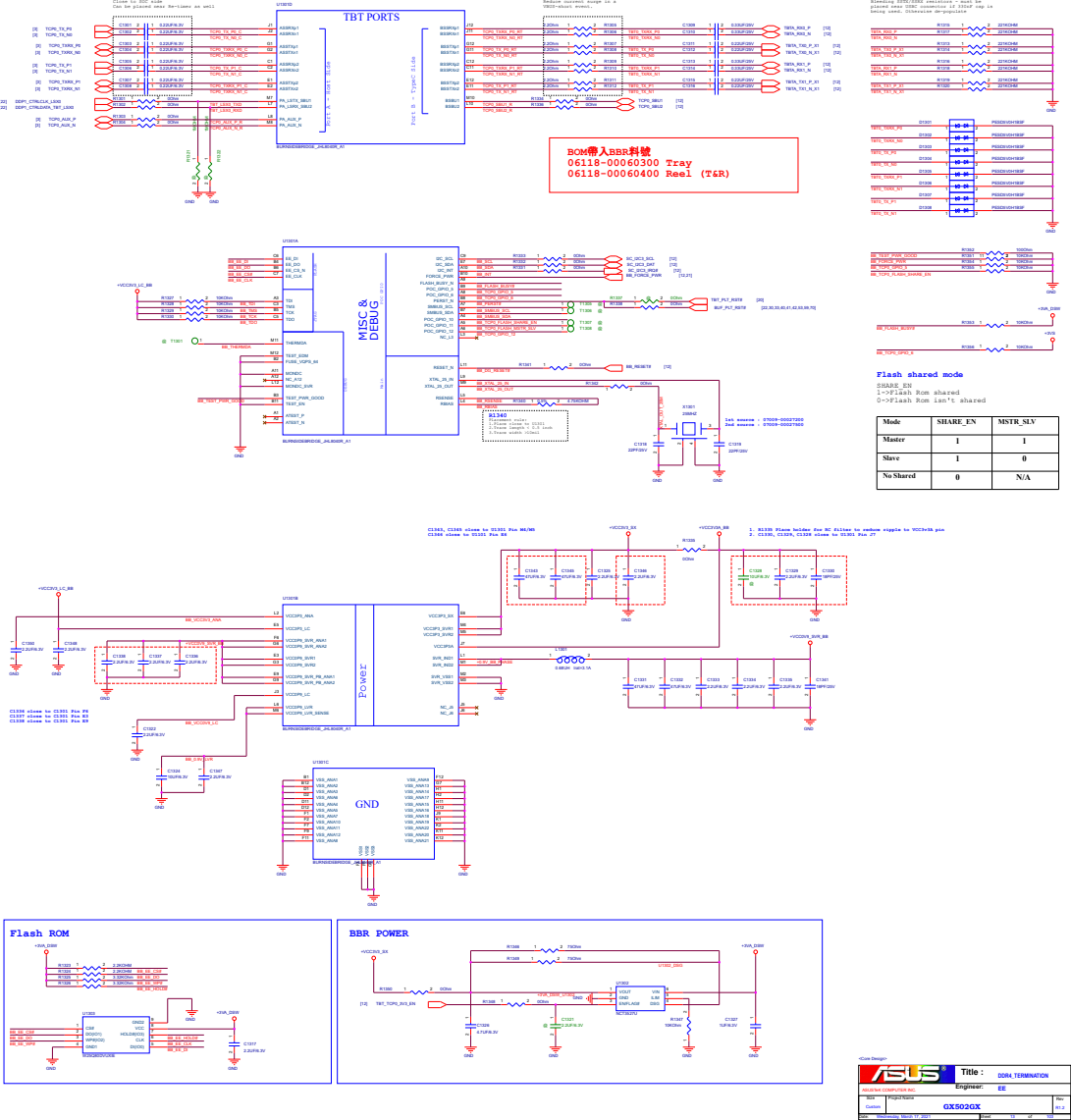


Decoupling Solution						
Power Rail		Decap Placement	Form Factor	Value	Number	Note
RVP REV1p0	VCCIN_AUX	CPU Primary Side	7343	330uF	2	
			0603	47uF	4	
		CPU Secondary side	0402	10uF	6	
			0603	47uF	8	
		PCH Primary Side	0603	47uF	7	5上2下 上 (TGL-H RVP MPI SOCKET STUFFING)
			0402	10uF	4	(TGL-H RVP MPI SOCKET STUFFING)
			0603	22uF	6	4上2下 上 (TGL-H RVP MPI SOCKET STUFFING)
		PCH Secondary Side	0402	10uF	4	4下上件 (TGL-H RVP MPI SOCKET STUFFING)
			0603	22uF	4	4下上件 (TGL-H RVP PPV SOCKET STUFFING)

Decoupling Solution						
Power Rail		Decap Placement	Form Factor	Value	Number	Note
BEP REV0p7	VCCIN_AUX	CPU Primary Side	7343	330uF	2	
			0603	47uF	4	
		CPU Secondary side	0402	10uF	6	
			0603	47uF	8	
		PCH Primary Side	0603	47uF	5	
			0402	10uF	4	

Decoupling Solution						
Power Rail		Decap Placement	Form Factor	Value	Number	Note
目前線路	VCCIN_AUX	CPU Primary Side	7343	220uF	1	
			3528	330uF	2	1下上件1上件
			0603	47uF	6+6	
		CPU Secondary side	0402	10uF	6	
			0603	22uF	17+6	17上4下上
		PCH Primary Side	7343	470uF	1	
			0603	22uF	10	1上3下上

ASUS	Project Name: GX502GX		Rev: 01.2
Title : CPU_PWR			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 0 of 103		

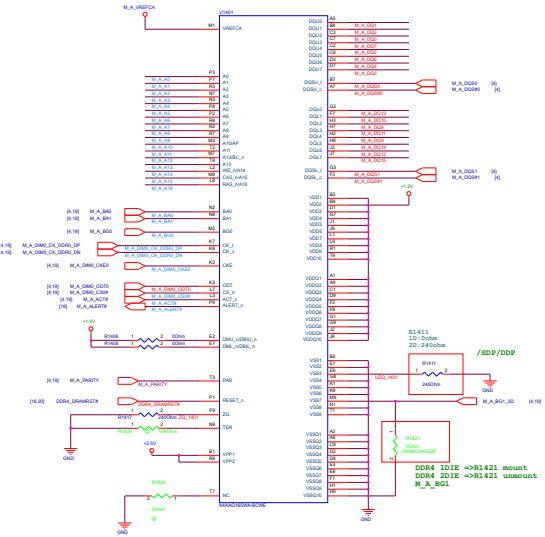

TBT PORTS
MISC & DEBUG
Power
GND
Flash ROM
BBR POWER
BOM導入BBR料號
06118-00060300 Tray
06118-00060400 Reel (T&R)
Flash shared mode
SHARE_EN
1->Flash Rom shared
0->Flash Rom isn't shared
Mode | SHARE_EN | MSTR_SLV
Master | 1 | 1
Slave | 1 | 0
No Shared | 0 | N/A
Title : DDR4_TERMINATION
Engineer: EE
GX5020X

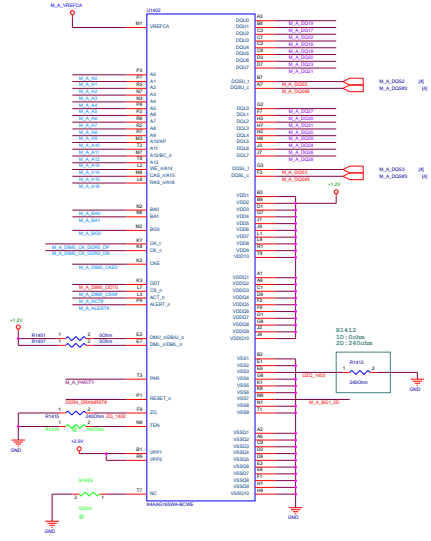
DQS0~DQS1(DQ0~DQ15)

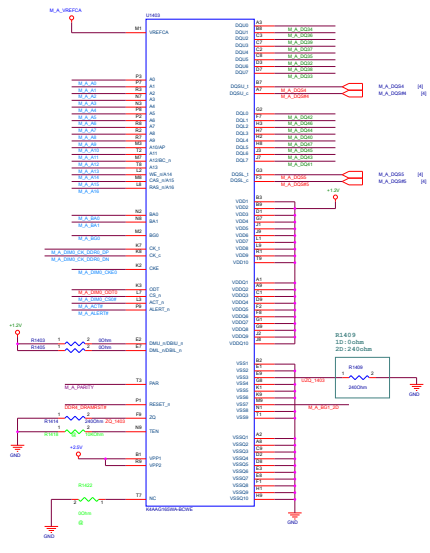
DQS2~DQS3(DQ16~DQ31)

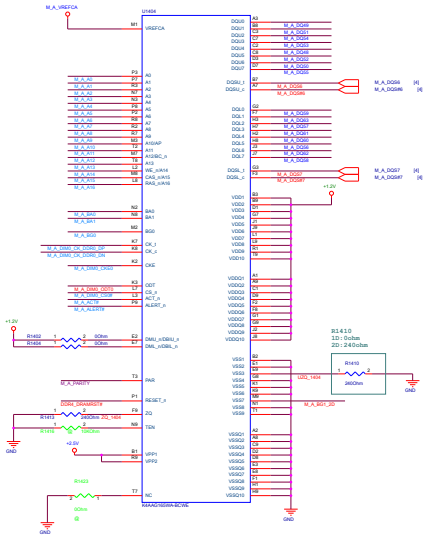
DQS4~DQS5(DQ32~DQ47)

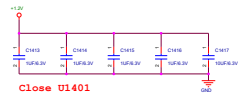
DQS6~DQS7(DQ48~DQ63)

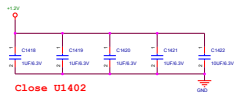


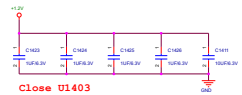


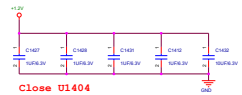


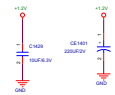


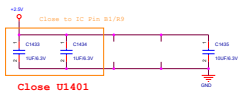


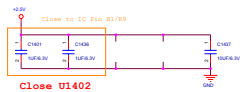


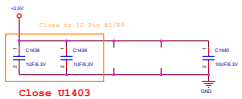


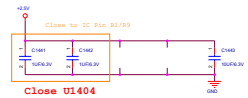


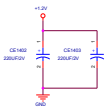








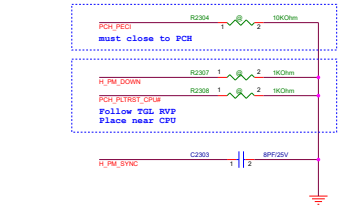


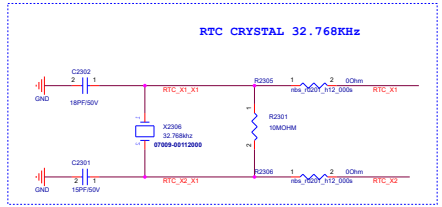


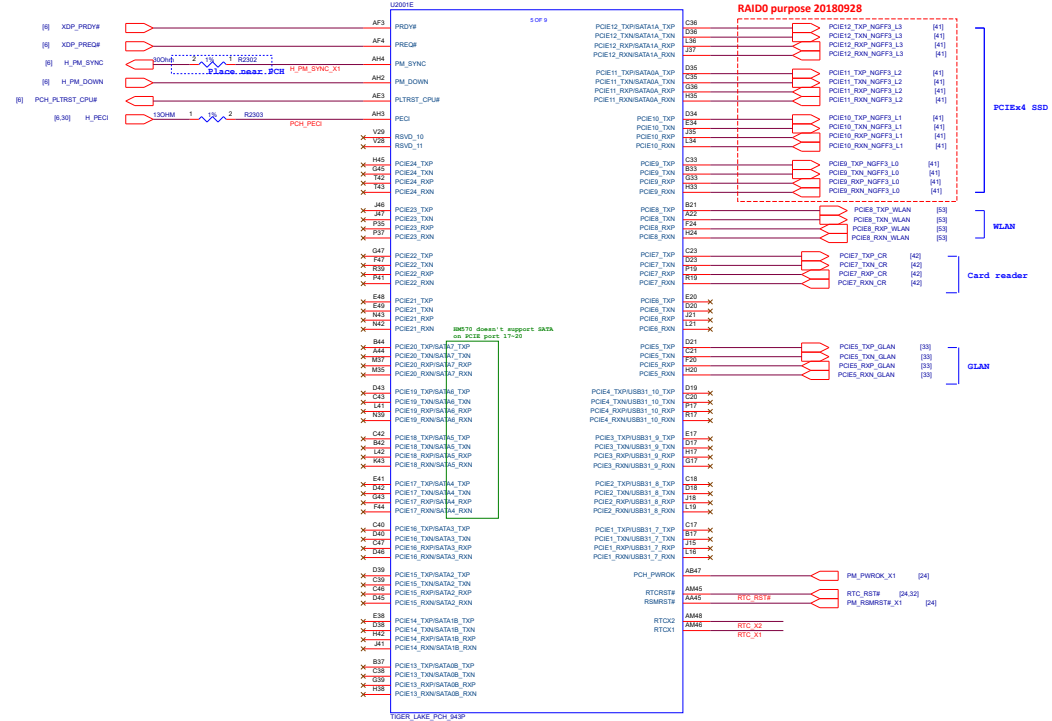
<Core Design>
ASUSTeK COMPUTER INC.
Title : DDR4_ON-BOARD_A1
Engineer: EE
Size: D
Project Name: GX502GX
Rev: R1.2
Date: Wednesday, March 17, 2021
Sheet 14 of 103

PCIE Setting

PCIE Controller	HSIO Capabilities	Function
1	PCIE#01 - USB3.1#07	
	PCIE#02 - USB3.1#08	
	PCIE#03 - USB3.1#09	
	PCIE#04 - USB3.1#10	
2	PCIE#05	GLAN
	PCIE#06	
	PCIE#07	
	PCIE#08	WLAN
3	**PCIE#09**	**PCIE 9_SSD_LAN0**
	PCIE#10	**PCIE10_SSD_LAN1**
	PCIE#11- SATA-0a	**PCIE11_SSD_LAN2**
	PCIE#12- SATA-1a	**PCIE12_SSD_LAN3**
4	PCIE#13- SATA-0b	**PCIE13_Card Reader**
	PCIE#14- SATA-1b	
	PCIE#15 / SATA#2	
	PCIE#16 / SATA#3	
5	**PCIE#17 / SATA#4**	**PCIE21_SSD_LAN0/SATA4**
	PCIE#18 / SATA#5	**PCIE22_SSD_LAN1**
	PCIE#19 / SATA#6	**PCIE23_SSD_LAN2**
	PCIE#20 / SATA#7	**PCIE24_SSD_LAN3**
6	**PCIE#21**	
	PCIE#22	
	PCIE#23	
	PCIE#24	







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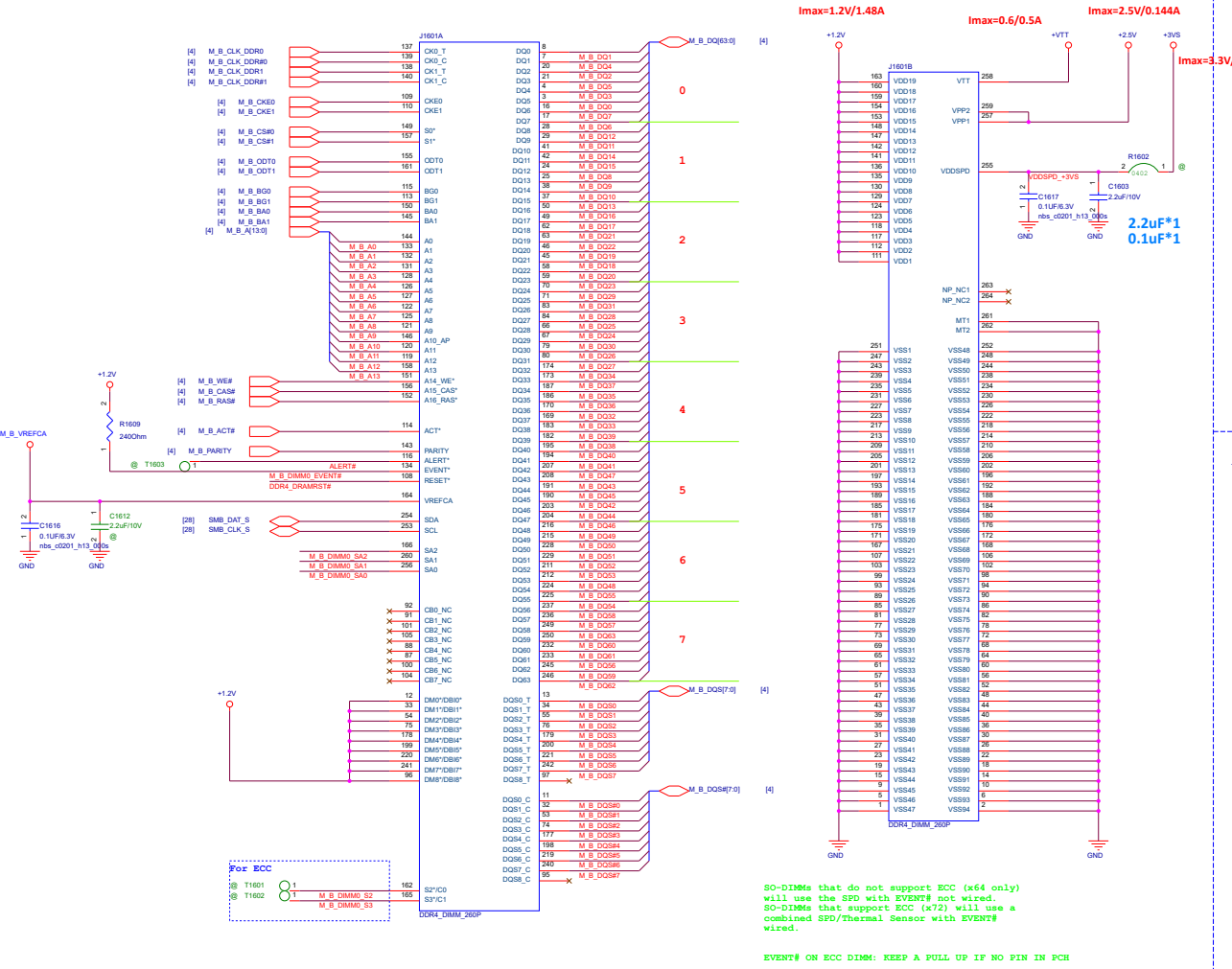
Flex I/O Lane	SKU		
	HM570	WM590	QM580
0	USB 3.2 Gen 2x1 #1	USB 3.2 Gen 2x1 #1	USB 3.2 Gen 2x1 #1
1	USB 3.2 Gen 2x1 #2	USB 3.2 Gen 2x1 #2	USB 3.2 Gen 2x1 #2
2	USB 3.2 Gen 2x1 #3	USB 3.2 Gen 2x1 #3	USB 3.2 Gen 2x1 #3
3	USB 3.2 Gen 2x1 #4	USB 3.2 Gen 2x1 #4	USB 3.2 Gen 2x1 #4
4	USB 3.2 Gen 2x1 #5	USB 3.2 Gen 2x1 #5	USB 3.2 Gen 2x1 #5
5	USB 3.2 Gen 2x1 #6	USB 3.2 Gen 2x1 #6	USB 3.2 Gen 2x1 #6
6	USB 3.2 Gen 2x1 #7, PCIe #1	USB 3.2 Gen 2x1 #7, PCIe #1	USB 3.2 Gen 2x1 #7, PCIe #1
7	USB 3.2 Gen 2x1 #8, PCIe #2	USB 3.2 Gen 2x1 #8, PCIe #2	USB 3.2 Gen 2x1 #8, PCIe #2
8	USB 3.2 Gen 1x1 #9, PCIe #3	USB 3.2 Gen 1x1 #9, PCIe #3	USB 3.2 Gen 1x1 #9, PCIe #3
9	USB 3.2 Gen 1x1 #10, PCIe #4	USB 3.2 Gen 1x1 #10, PCIe #4	USB 3.2 Gen 1x1 #10, PCIe #4
10	PCIe #5, GbE	PCIe #5, GbE	PCIe #5, GbE
11	PCIe #6	PCIe #6	PCIe #6
12	PCIe #7	PCIe #7	PCIe #7
13	PCIe #8	PCIe #8	PCIe #8
14	DMI #7	DMI #7	DMI #7
15	DMI #6	DMI #6	DMI #6
16	DMI #5	DMI #5	DMI #5
17	DMI #4	DMI #4	DMI #4
18	DMI #3	DMI #3	DMI #3
19	DMI #2	DMI #2	DMI #2
20	DMI #1	DMI #1	DMI #1

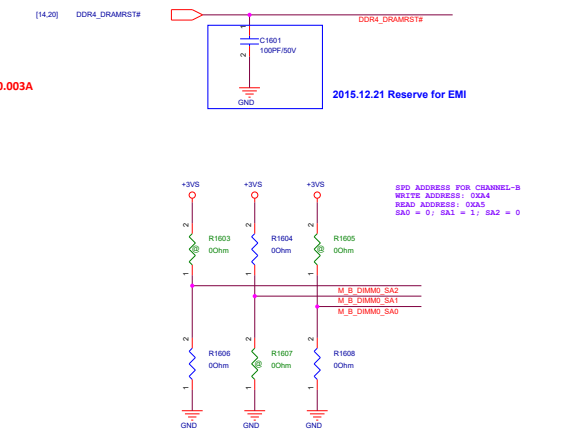
continued...

Flex I/O Lane	SKU		
	HM570	WM590	QM580
21	DMI #0	DMI #0	DMI #0
22	PCIe #9, GbE, TSN	PCIe #9, GbE, TSN	PCIe #9, GbE, TSN
23	PCIe #10, TSN	PCIe #10, TSN	PCIe #10, TSN
24	PCIe #11, SATA #0A	PCIe #11, SATA #0A	PCIe #11, SATA #0A
25	PCIe #12, SATA #1A, GbE	PCIe #12, SATA #1A, GbE	PCIe #12, SATA #1A, GbE
26	PCIe #13, SATA #0B, GbE	PCIe #13, SATA #0B, GbE	PCIe #13, SATA #0B, GbE
27	PCIe #14, SATA #1B	PCIe #14, SATA #1B	PCIe #14, SATA #1B
28	PCIe #15, SATA #2	PCIe #15, SATA #2	PCIe #15, SATA #2
29	PCIe #16, SATA #3	PCIe #16, SATA #3	PCIe #16, SATA #3
30	PCIe #17, SATA #4	PCIe #17, SATA #4	PCIe #17, SATA #4
31	PCIe #18, SATA #5	PCIe #18, SATA #5	PCIe #18, SATA #5
32	PCIe #19 / Intel® RST for PCIe Storage Port, SATA #6	PCIe #19 / Intel® RST for PCIe Storage Port, SATA #6	PCIe #19 / Intel® RST for PCIe Storage Port, SATA #6
33	PCIe #20 / Intel® RST for PCIe Storage Port, SATA #7	PCIe #20 / Intel® RST for PCIe Storage Port, SATA #7	PCIe #20 / Intel® RST for PCIe Storage Port, SATA #7
34	PCIe #21	PCIe #21	PCIe #21
35	PCIe #22	PCIe #22	PCIe #22
36	PCIe #23	PCIe #23	PCIe #23
37	PCIe #24	PCIe #24	PCIe #24

ASUS	Project Name: GX502GX		Rev: R1.2
Title :	PCH-CPT(2)_PCIE,CLK,USB		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 23 of 103		

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)





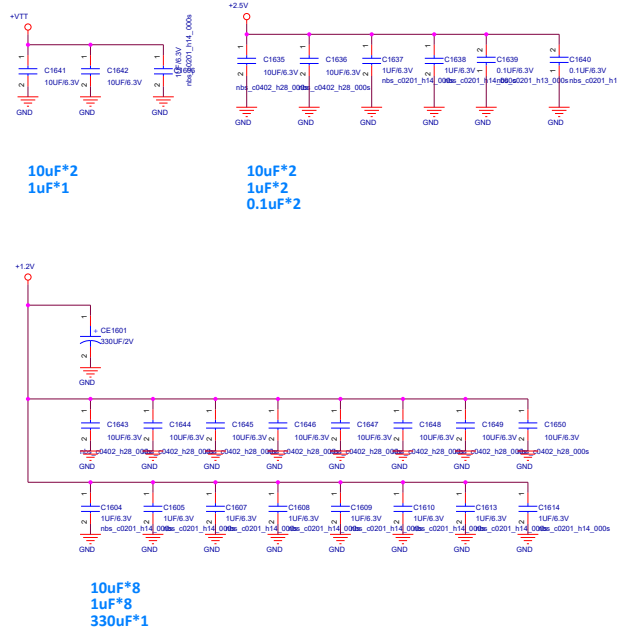


Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

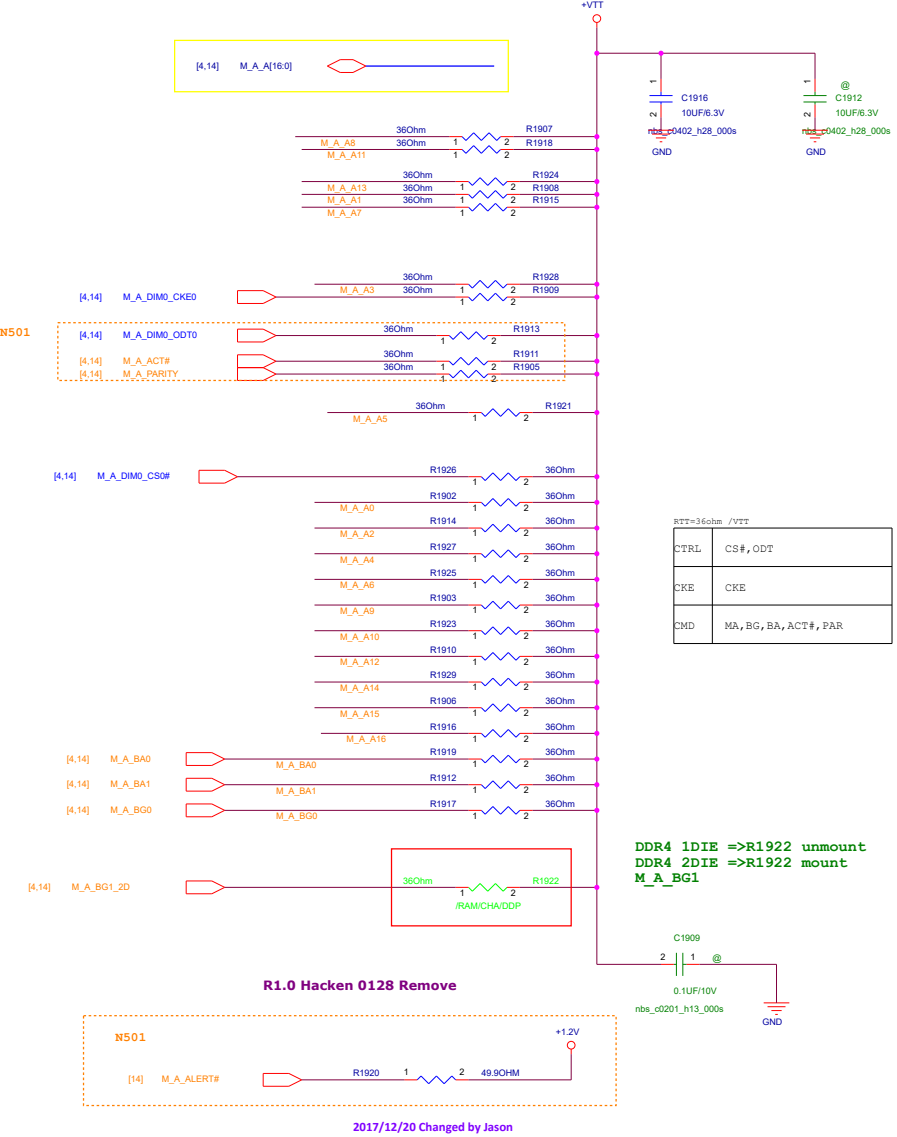
DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051800
2nd : Samsung - 03A08-00051700
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061900
2nd : Samsung - 03A08-00061800

Project Name: GX502GX		Rev: R1.2
Title : DIM_DDR4 SO-DIMM B1		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 16 of 103	

Main Board

2017/12/05 Remove TBT_I2C_SCL_PCH/TBT_I2C_SDA_PCH by James

ASUS	Project Name: GX502GX	Rev: R1.2
Title : PCH-CPT(6)_GPIO,MISC		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 25 of 103	



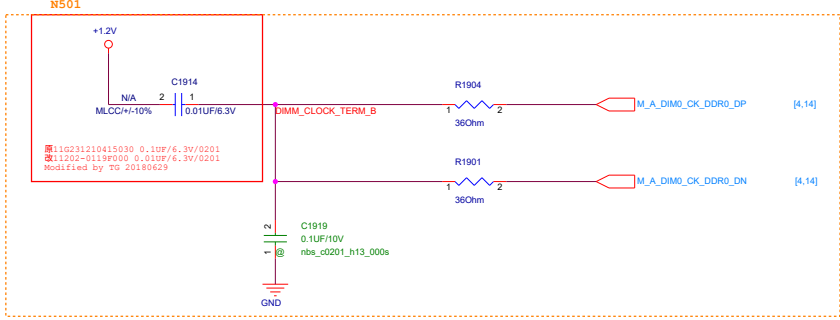
RTT=36ohm /VTT

CTRL	CS#,ODT
CKE	CKE
CMD	MA,BG,BA,ACT#,PAR

DDR4 1DIE =>R1922 unmount
DDR4 2DIE =>R1922 mount
M_A_BG1

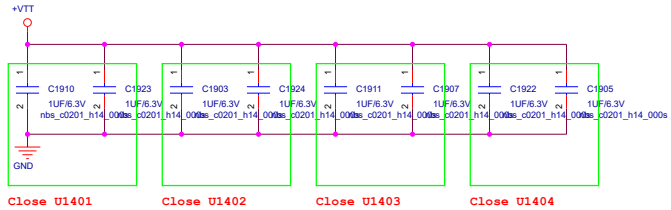
R1.0 Hacken 0128 Remove

2017/12/20 Changed by Jason



Clock Pull up power change from +0.6V to +1.2V (CFL PDG) 20820601

10uF*2
1uF*8



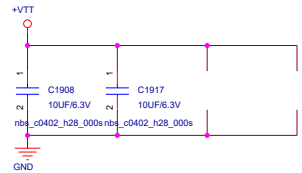


Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

<Core Design>

ASUSTeK COMPUTER

Title : *****

Engineer: EE

Size	Project Name	Rev
Custom	GX502GX	R1.2

Date: Wednesday, March 17, 2021 Sheet 19 of 103

Imax=2port+2CC=6.43A

Imax=100mA

Connect to EC

Connect to PCH

Connect to I2C ROM & BB & 1205

SN29010ZYBGR

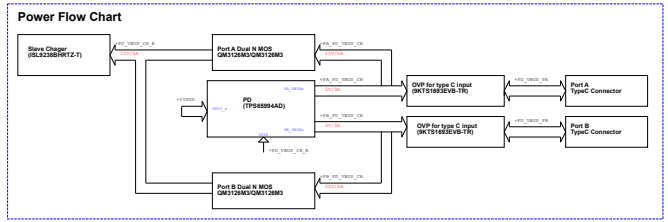
I2C EC Slave Address -> 0x42(W) (Port0)
I2C EC Slave Address -> 0x44(W) (Port1)

I2C ROM address 0xA0(W)

UX435 ER
for 3VA_DSW leakage

Q1202,Q1203只用07005-00660200與07005-00950000

Power Flow Chart



From TBT BB
From PD
To ConnectorA

From 1205A
From PD
To ConnectorB

Port A Dual N MOS

Port B Dual N MOS

TYPE-C Connector

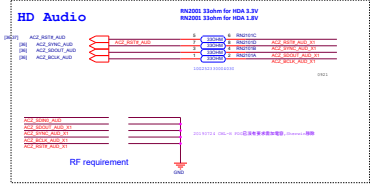
Close to typeC connector(A4/A9/B4/B9)

ASUS	Project Name: GX703_GTi603		Rev: 00.xx
Title: TBT_TPS65993AD67type C			
Size:	Dept.: Mobile Com/NBSBU	Engineer: EE4	
Date: Wednesday, March 27, 2019	Sheet:	of:	100

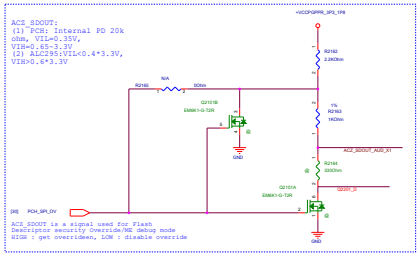
	Function	PCIe* Gen1/2/3 support	PCIe* Gen4 support
CLKREQ-0	**GPU**	**V**	**V**
CLKREQ-1		**V**	
CLKREQ-2	**WLAN**	**V**	
CLKREQ-3		**V**	**V**
CLKREQ-4		**V**	**V**
CLKREQ-5		**V**	
CLKREQ-6	**PCH SSD1**	**V**	
CLKREQ-7	**CPU SSD3**	**V**	**V**
CLKREQ-8	**GLAN**	**V**	
CLKREQ-9	**Card Reader**	**V**	**V**
CLKREQ-10~15		**V**	

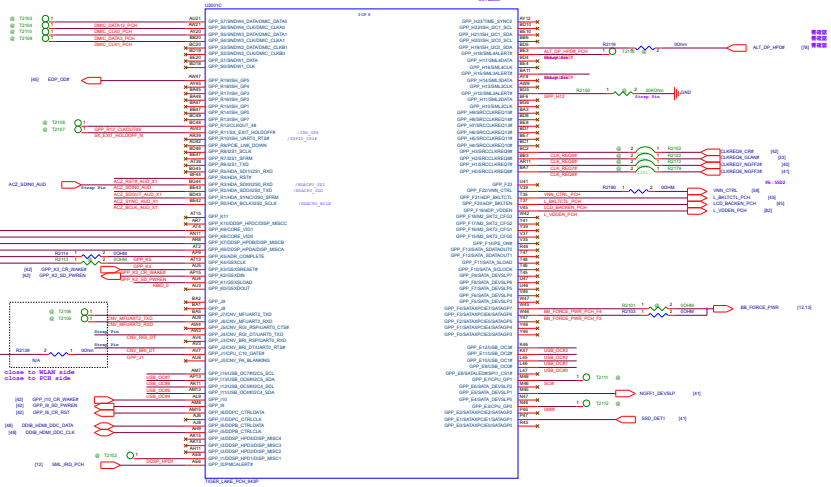
Project Name	GX502GX		Rev R1.2
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR		
Size Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 20	of 103	

ASUS	Project Name: GX502GX	Rev: R1.2
Title : TEST POINT		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 29 of 103	



	Function	PCIe* Gen1/2/3 support	PCIe* Gen4 support
CLKREQ-0	GPU	V	V
CLKREQ-1		V	
CLKREQ-2	WLAN	V	
CLKREQ-3		V	V
CLKREQ-4		V	V
CLKREQ-5	PCH SSD1	V	
CLKREQ-6		V	
CLKREQ-7	CPU SSD3	V	V
CLKREQ-8	GLAN	V	
CLKREQ-9	Card Reader	V	V
CLKREQ-10~15		V	

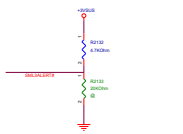




Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	
		+3VS		

Strap pin

Strap => JTAG ODT



PCH_GPPH15: weak internal pull down	
PU	**JTAG ODT is enabled<>**
PD	JTAG ODT is disabled

Strap => VCCSPI configuration

PCH_GPPH18:weak internal pull down	
PU	VCCSPI at 1.8 V
PD	**VCCSPI at 3.3 V(Default)<>**

Strap => XTAL Frequency Selection

PCH_GPPJ2: weak internal pull down	
PU	24 MHz
PD	**38.4 MHz (default)<>**

Strap => M.2 CNVi Mode Select

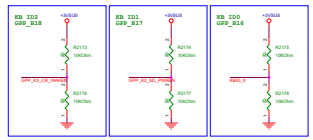
GPP_J4/CNV_BGI_DT1:
This strap board can have an internal pull-up or pull-down.
A weak external pull-up is required.
0=Integrated CNVi enabled.
1=Integrated CNVi disabled
If the CNVi device's CRF chip is connected to the PCH CNVi interface,
the device internal pull-down resistor
will pull the strap low to enable CNVi interface.

PCH_GPPJ4: no internal pull up and pull down	
PU	Integrated CNVi disabled
PD	**Integrated CNVi enable<>**

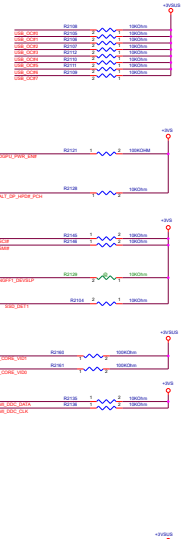
Strap => eSPI Flash Sharing Mode

PCH_GPP_H12: weak internal pull down

PCH_GPPH12: weak internal pull down	
PU	Slave Attached Flash Sharing (SAFS) enabled
PD	**Master Attached Flash Sharing (MAFS) enabled (Default)<>**



KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向				
Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H



Strap pin

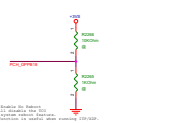
Strap -> eSPI or LPC

PCH_GPPC5: weak internal pull down	
PU	Disable eSPI
PD	**Enable eSPI (default)<>**

Strap -> Top Swap Override

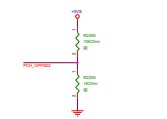
PCH_GPP_B14: weak internal pull down	
PU	Enable
PD	**Disable (default)<>**

Strap -> No Reboot



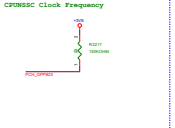
PCH_GPP_B18: weak internal pull down	
PU	Enable
PD	**Disable (default)<>**

Strap -> Boot BIOS Strap Bit BBS



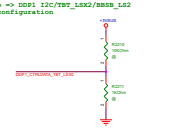
PCH_GPP_B22: weak internal pull down	
PU	BIOS Fetches are routed to the eSPI Peripheral Channel
PD	**BIOS Fetches are routed to SPI (BAF) or the eSPI Flash Channel (SAF)<>**

Strap -> CPUNSSC Clock Frequency



PCH_GPP_B23: weak internal pull down	
PU	19.2MHz
PD	**38.4MHz (default)<>**

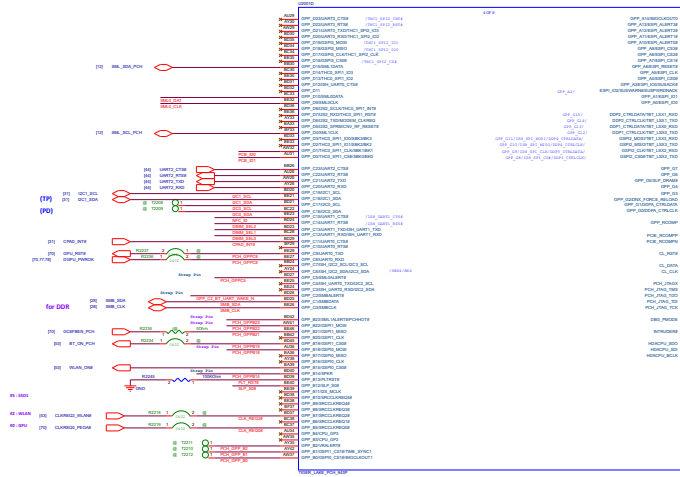
Strap -> DDI I2C/TBT_LSX2/BBSB_LS2 VCC configuration



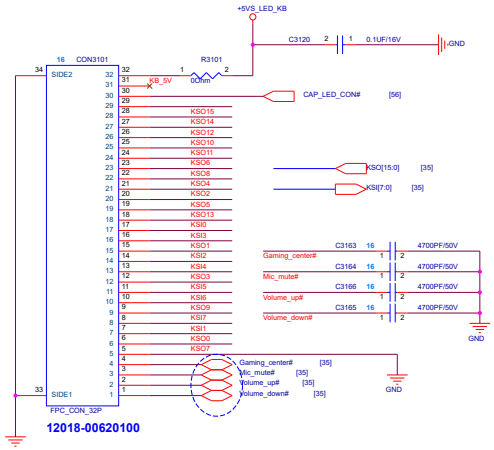
PCH_GPP_G13: weak internal pull down	
PU	DDPI I2C/TBT_LSX2/BBSB_LS2 at 3.3V
PD	**DDPI I2C/TBT_LSX2/BBSB_LS2 at 1.8V**

20190729 Sharein Follow CNL-H Reference Schematic Modify

PCH_GPPC2: weak internal pull down	
PU	**Enable Intel ME Crypto Transport Layer Security(TLS) cipher suite (no confidentiality). (Default) Must be pulled up to support Intel® AMT with TLS.<>**
PD	Disable Intel ME Crypto Transport Layer Security(TLS) cipher suite (no confidentiality). (Default)

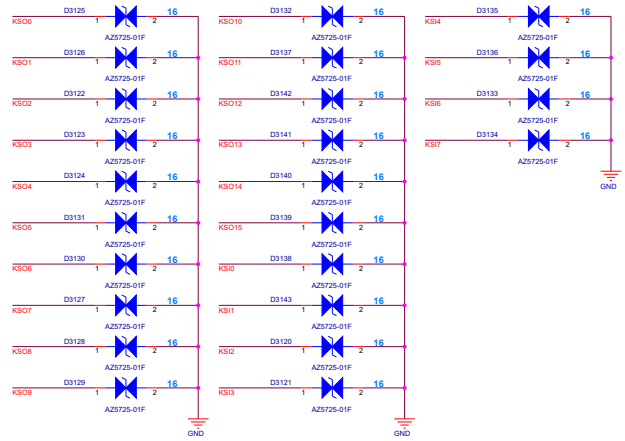

U2000/10
eSPI
SMB_SDA_PCH
SMB_SCL_PCH
(TP)
(PD)
I2C1_SCL
I2C1_SDA
CPND_INT#
GPU_RST#
DGPU_PWROK
for DDR
SMB_SDA
SMB_CLK
DGPWRTN_PCH
RT_ON_PCH
WLAN_ON#
CLKREQ2_WLAN#
CLKREQ0_PEG#
Strap Pin
PCH_GPPC5
PCH_GPP_B14
PCH_GPP_B18
PCH_GPP_B22
PCH_GPP_B23
PCH_GPP_G13
PCH_GPP_B2
PCH_GPP_B1
PCH_GPP_B0
Do not set GPP_G2 to native function.
PCIE RCOMP 100 OHM 1%
PCH_RCOMP
PCH_ZVM
PCH_ZVP
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
PCH_JTAG_TMS
CNVI_PMODE
INTRUDER#
HDACPCI_SDO
HDACPCI_SDI
HDACPCI_BCLK
SUSCLK
SLP_SUS#
SLP_S0#
PLT_RST#
RTCRST#
SRTCRST#
SPKR
SUS_STAT#
SUSWARN#
SUSACK#
SLP_A#
SLP_S3#
SLP_S4#
SLP_LAN#
SLP_WLAN#
SLP_S5#
WAKE#
PWRBTN#
ACPRESENT
BATLOW#
PLTRST#
SYS_RESET#
MEPWROUT#
CPUPWRGD
THRMTRIP#
PROCPWRGD
CATERR#
SKTOCC#
PECI
PROCHOT#
MEMHOT#
PMSYNCH
VRALERT#
CPU_C10_GATE#
PCH_PWROK
SYS_PWROK
DSW_PWROK
RSMRST#

Keyboard Connector(GU603)



12018-00620100

For EMI



For EMI

Keyboard Connector(GX703)

Keyboard Backlight

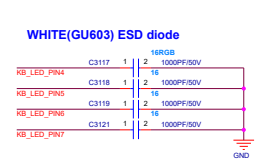
Perkey(GX703)

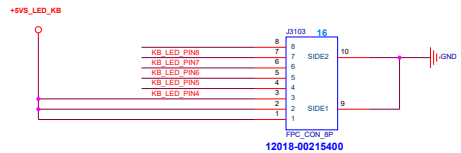
光軸Perkey BD	function key
IT8298	IT8237

Keyboard Backlight

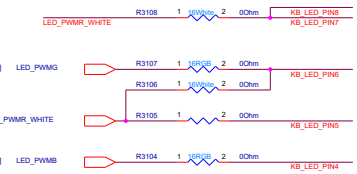
One Zone(GU603)

WHITE(GU603) ESD diode



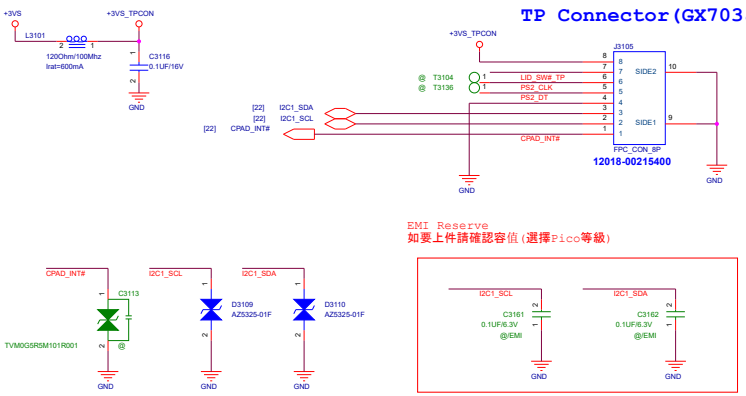


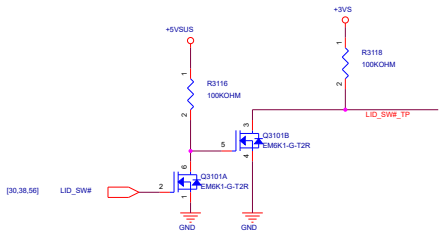
12018-00215400



	White	RGB
PIN 8	White	NC
PIN 7	White	NC
PIN 6	White	Cathode LED1 Green
PIN 5	White	Cathode LED1 Red
PIN 4	NC	Cathode LED1 Blue
PIN 3	VCC	VCC Blue
PIN 2	VCC	VCC Red
PIN 1	VCC	VCC Green

TP Connector(GX703&GU603)





<Core Design>

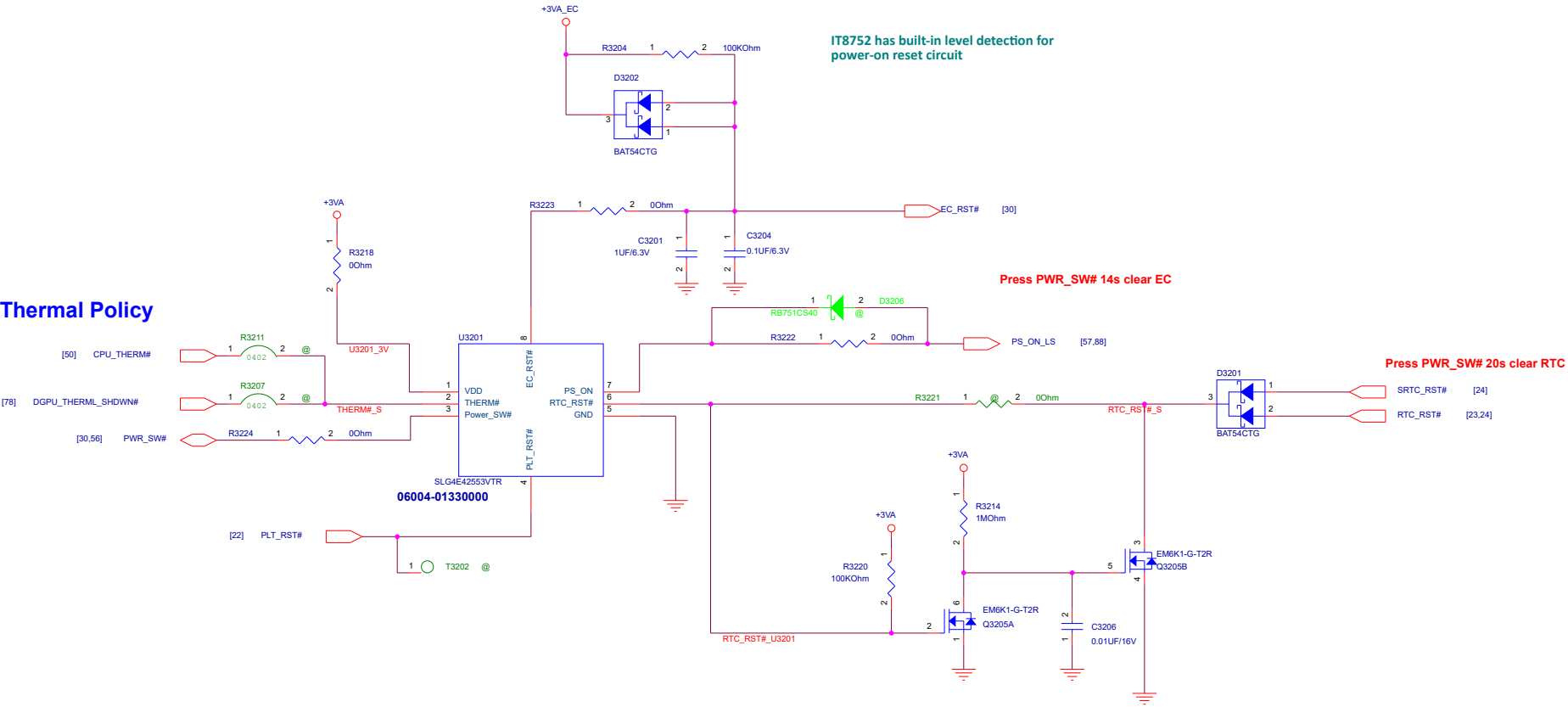
ASUSTeK COMPUTER

Title : KBC_KB & TP

Engineer: EE

Size	Project Name	Rev
Custom	GX502GX	R1.2

Date: Wednesday, March 17, 2021 Sheet 31 of 103



<Core Design>

ASUSTeK COMPUTER	Title : RST_Reset Circuit	
	Engineer: EE	
Size: Custom	Project Name: GX502GX	Rev: R1.2
Date: Wednesday, March 17, 2021	Sheet 32 of 103	

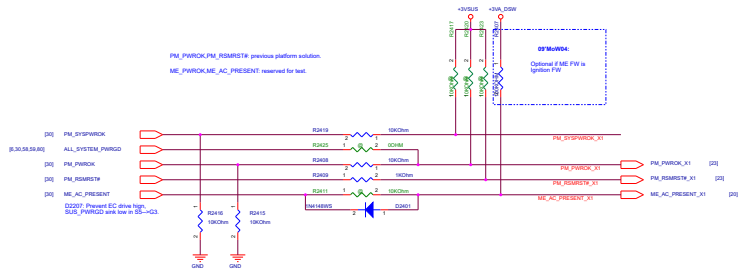
USB Setting

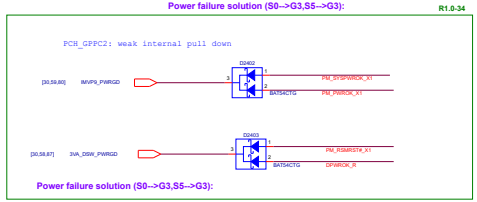
GX502GX USB Function define

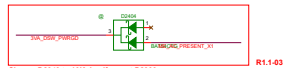
CNL HM370(only #1~#4 support GEN2)

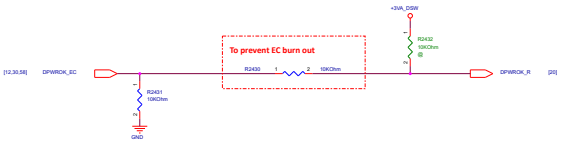
USB 2.0	Function
USB2_01	**(Port1)Thunderbolt**
USB2_02	
USB2_03	**(Port3)USB3.1 Gen1 TypeA**
USB2_04	**(Port1)USB3.1 Gen2 TypeA**
USB2_05	**(Port2)USB3.1 Gen1 TypeA**
USB2_06	
USB2_07	
USB2_05	
USB2_09	
USB2_10	**N key**
USB2_11	
USB2_12	
USB2_13	
USB2_14	**BT**

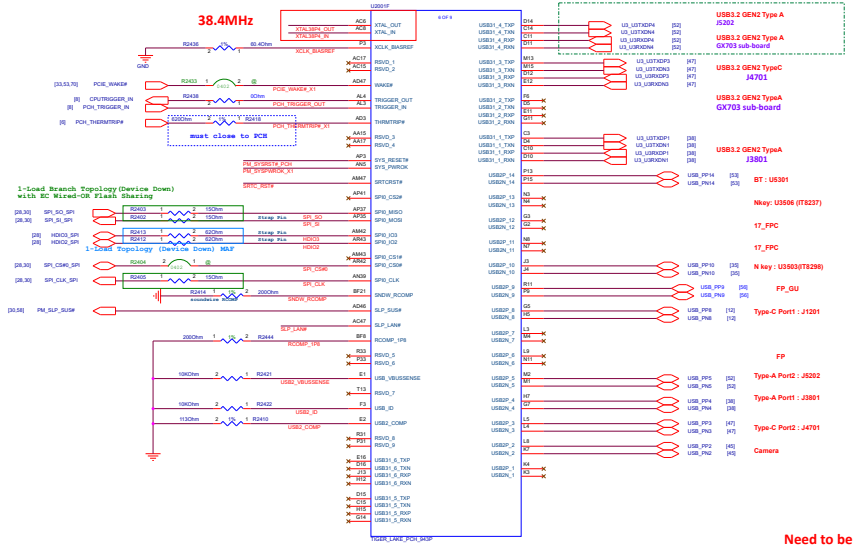
USB 3.1	Function
USB3.1#01	**(Port1)USB3.1 Gen2 TypeA**
USB3.1#02	**(Port2)USB3.1 Gen1 TypeA**
USB3.1#03	**(Port3)USB3.1 Gen1 TypeA**
USB3.1#04	
USB3.1#05	
USB3.1#06	
USB3.1#07	
USB3.1#08	

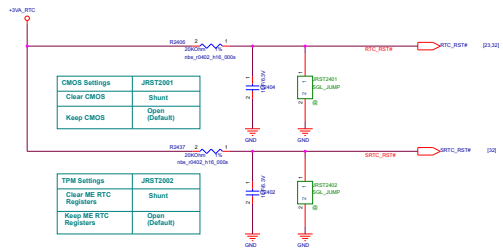


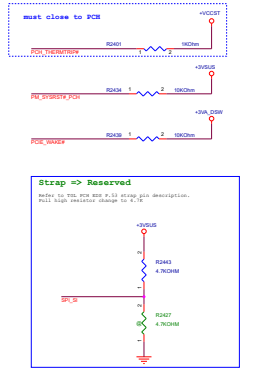




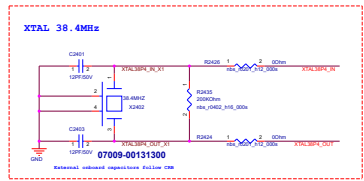






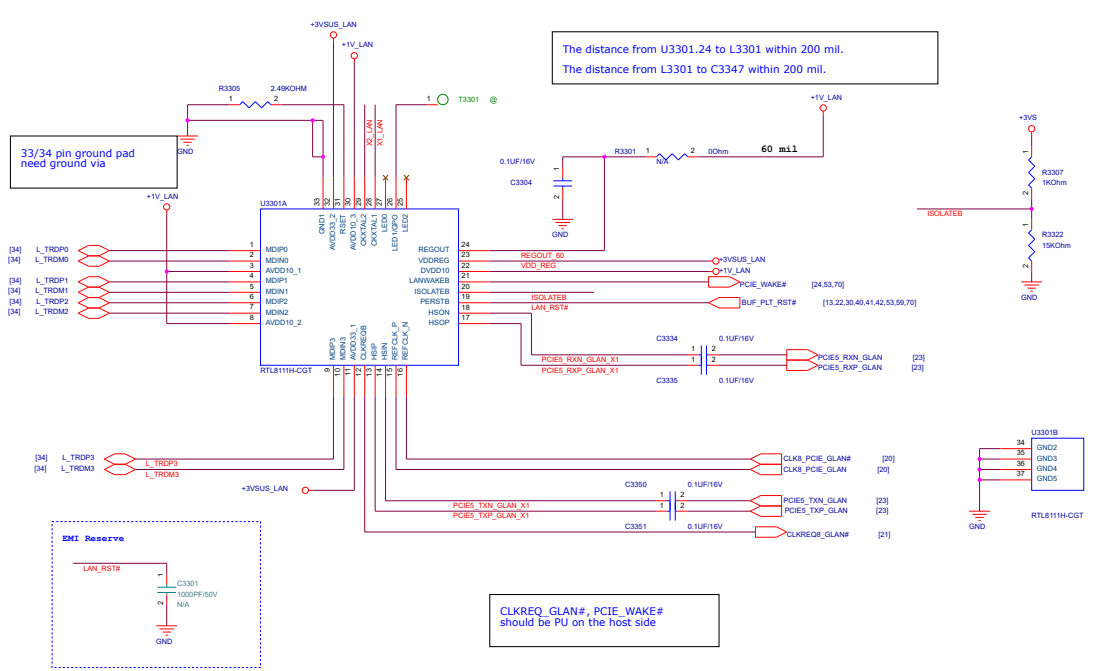


Need to be changed to a 38.4MHz crystal
Follow UX482

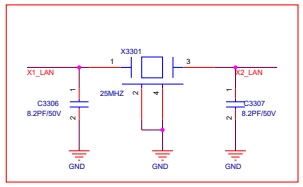


PCH	CPU	XTAL_IN/OUT Frequency
TGP-H	TGL-H	38.4 MHz
TGP-H	RLK-S	24 MHz

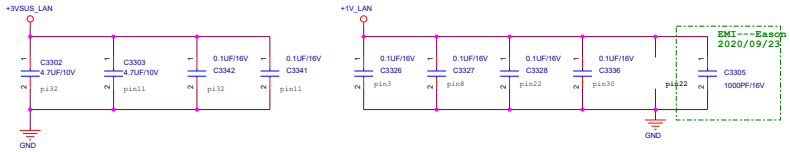
ASUS	Project Name	GX502GX	Rev 1.2
	Title :	PCH-CPT(4) eDP,PCI,DP	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 24 of 103		



Main Board



Realtek suggests 3V_LAN raise time >1ms



Project Name: GX502GX		Rev: R1.2
Title: LAN RTL8111GUX-CG		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 33 of 103	

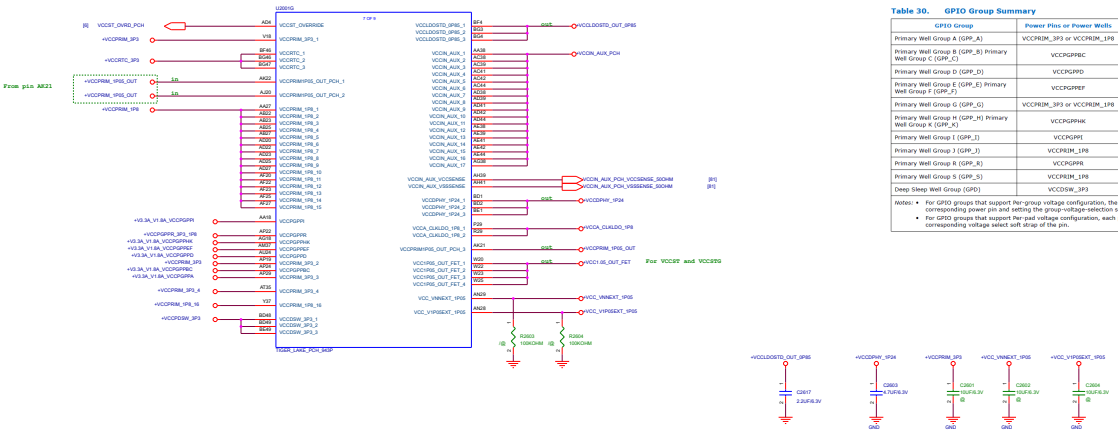


Table 30. GPIO Group Summary

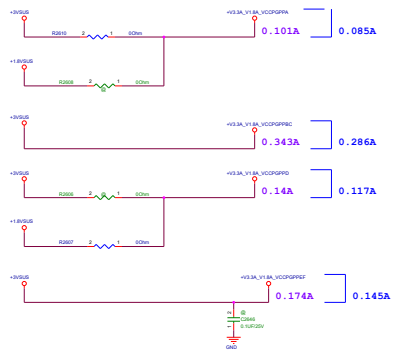
GPIO Group	Power Pins or Power Wells	Voltage
Primary Well Group A (GPP_A)	VCCPRIM_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group B (GPP_B) Primary Well Group C (GPP_C)	VCCPGPPBC	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group D (GPP_D)	VCCPGPPD	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group E (GPP_E) Primary Well Group F (GPP_F)	VCCPGPPEF	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group G (GPP_G)	VCCPRIM_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V (Per-pad voltage configuration)
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group I (GPP_I)	VCCPGPPI	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8 V Only
Primary Well Group R (GPP_R)	VCCPGPPR	1.8 V or 3.3 V (Per-group voltage configuration)
Primary Well Group S (GPP_S)	VCCPRIM_1P8	1.8 V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

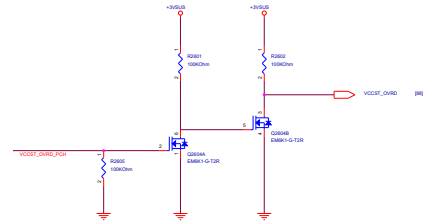
Notes:
- For GPIO groups that support Per-group voltage configuration, the voltage is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage.
- For GPIO groups that support Per-pad voltage configuration, each pin voltage is selected by setting the corresponding voltage select soft strap of the pin.

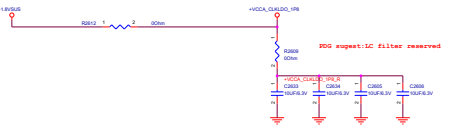
GPIO Voltage Level

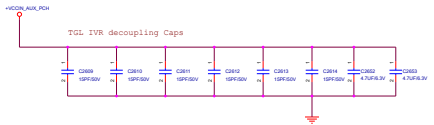
Group	Power pin	Power option	Power plane
GPP_A		1.8V or 3.3V	+3VSUS
GPP_B	VCCPGPPBC	1.8V or 3.3V	+3VSUS
GPP_C	VCCPGPPBC	1.8V or 3.3V	+3VSUS
GPP_D	VCCPGPPD	1.8V or 3.3V	+1.8VSUS
GPP_E	VCCPGPPEF	1.8V or 3.3V	+3VSUS
GPP_F	VCCPGPPEF	1.8V or 3.3V	+3VSUS
GPP_G		1.8V or 3.3V	+1.8VSUS
GPP_H	VCCPGPPHK	1.8V or 3.3V	+3VSUS
GPP_I	VCCPRIM_3P3	1.8V or 3.3V	+3VSUS
GPP_J		1.8V Only	+1.8VSUS
GPP_K	VCCPGPPHK	1.8V or 3.3V	+3VSUS
GPP_R	VCCPGPPR	1.8V or 3.3V	+1.8VSUS
GPP_S		1.8V Only	
GPD		3.3V Only	+3VA_DSW

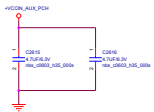
Per-group : GPP_B,GPP_C, GPP_D, GPP_E, GPP_F, GPP_H, GPP_I, GPP_K, and GPP_R
Per-pad : GPP_A,GPP_G

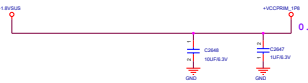




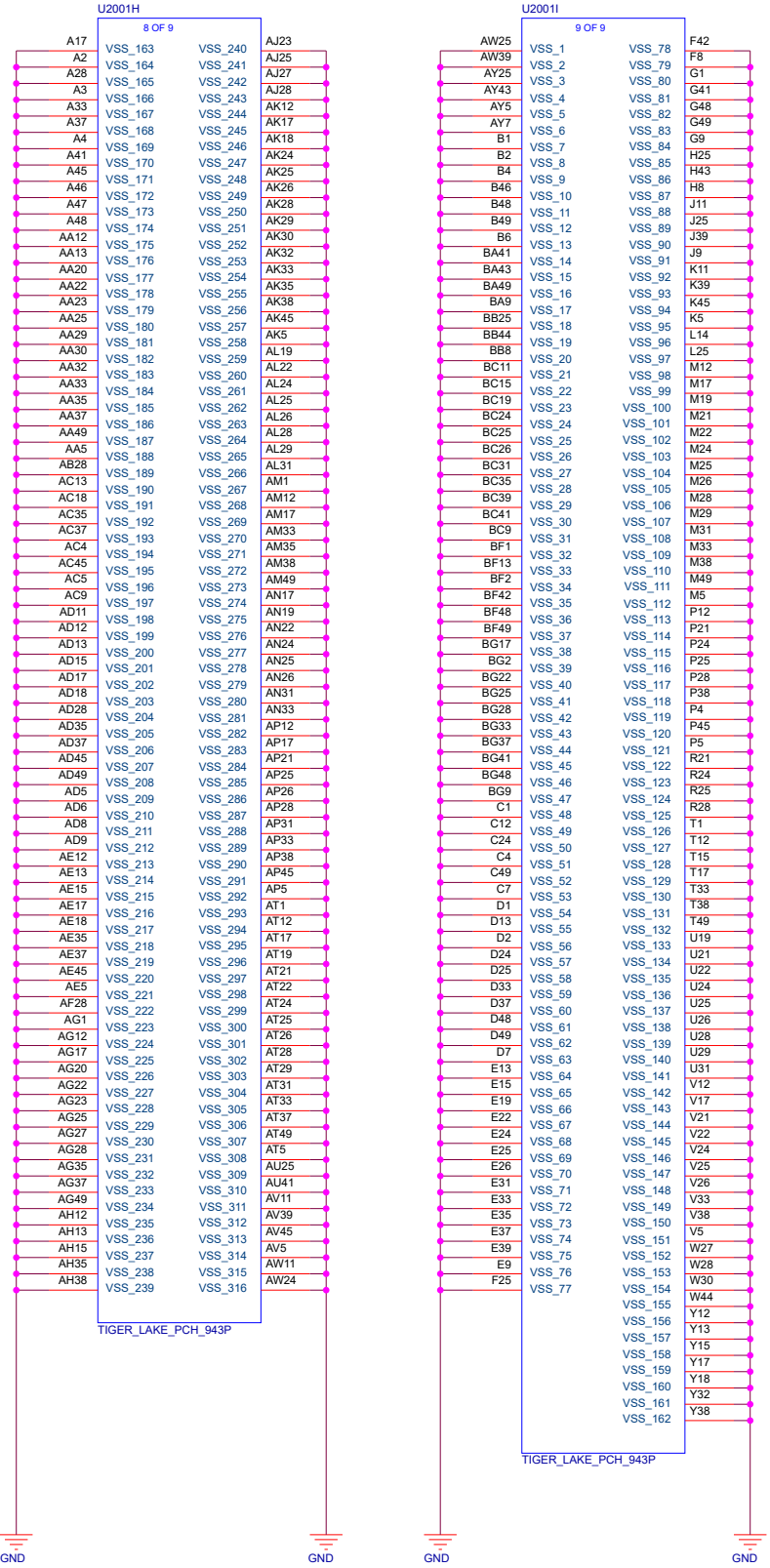








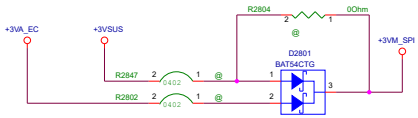
ASUS	Project Name: GX502GX		Rev: R1.2
Title : PCH-CPT(7)_POWER.GND			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 26 of 103		



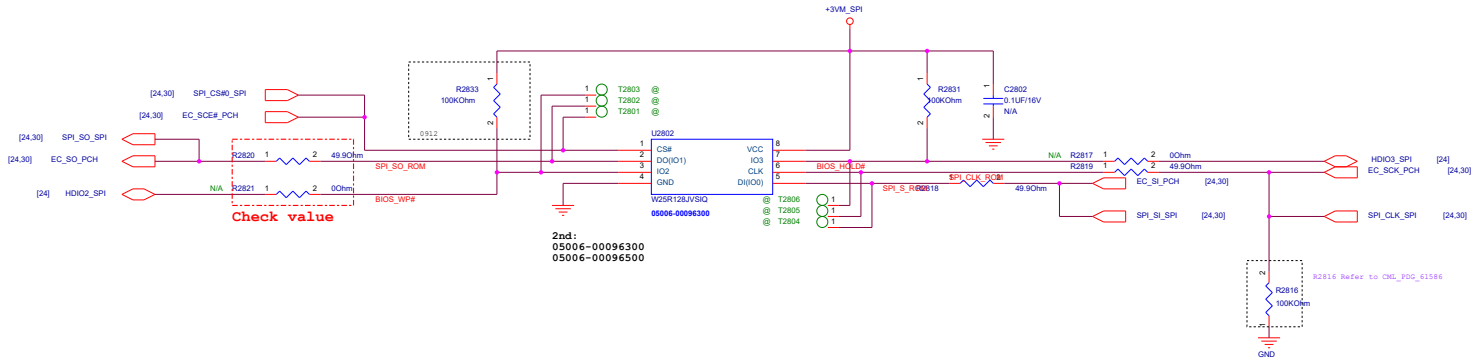
ASUS	Project Name: GX502GX	Rev: R1.2
Title :	PCH-CPT(8)_POWER,GND	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 27 of 103	

Main Board

SPI Power

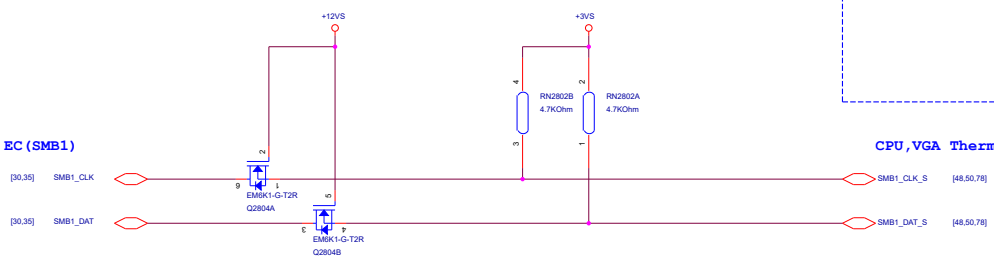


1st SPI ROM

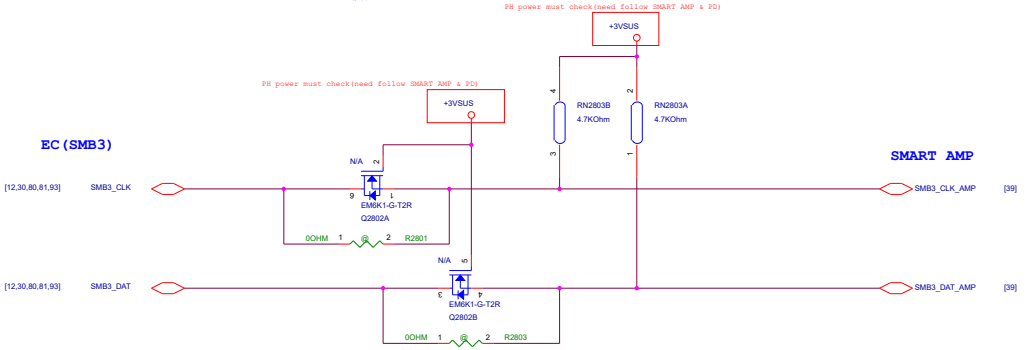


System Management Interface

EC(SMB1)



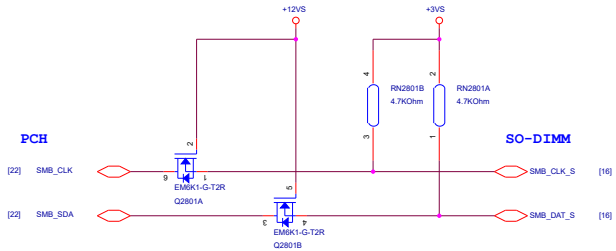
EC(SMB3)



CPU,VGA Thermal Sensor

SMART AMP

SMBus Interface



ASUS	Project Name: GX502GX		Rev: R1.2
Title : PCH-SPI ROM,OTH			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 28 of 103		

*** POWER

** [P.30] +3VA_EC

+3VA_EC

** [P.36] +1V8_AUD_DVDD_IO

+1V8_AUD_DVDD_IO

*** SINGAL

** Line to Codec [36]

[36] LINE1_R — LINE1_R

[36] LINE1_L — LINE1_L

** Headset from Codec [36]

[36] HPOUT_R — HPOUT_R

[36] HPOUT_L — HPOUT_L

[36] MIC2_VREFO_L — MIC2_VREFO_L

[36] MIC2_L_RING2 — MIC2_L_RING2

[36] MIC2_R_SLEEVE — MIC2_R_SLEEVE

[36] MIC2_VREFO_R — MIC2_VREFO_R

** Control Pin from Codec [36]

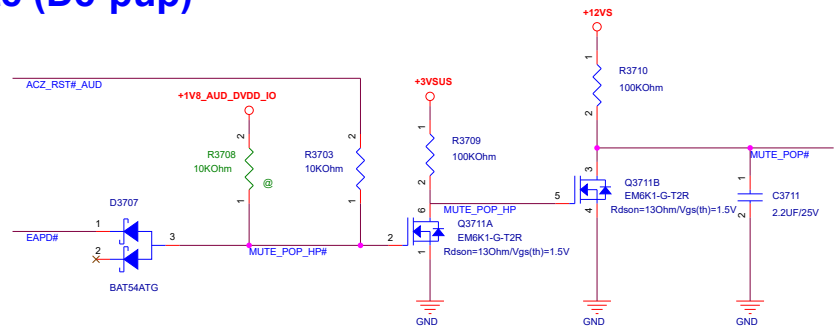
[36] EAPD# — EAPD#

[36] TOU_CON_L — TOU_CON_L

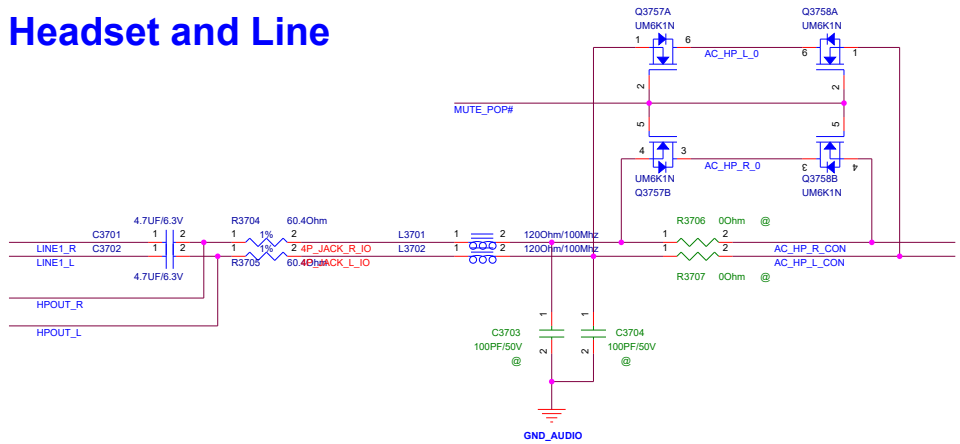
** Control Pin from APU [7]

[21,36] ACZ_RST#_AUD — ACZ_RST#_AUD

**Mute (De-pup)



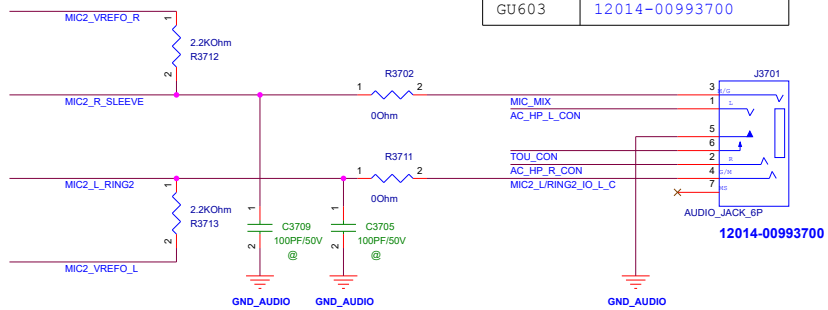
** Headset and Line



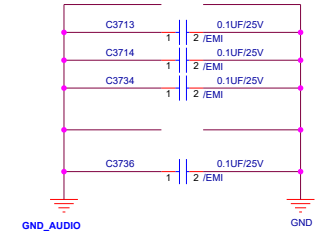
** Jack and MIC

** VBIAS Voltage from Codec [36]

GX703	12014-00993800
GU603	12014-00993700



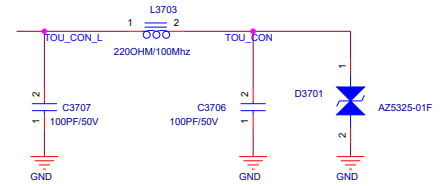
** A_GND / GND



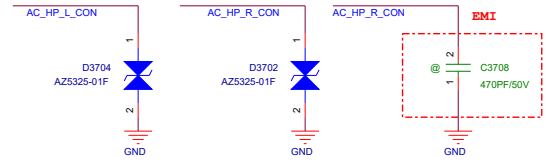
** TVS

teknisi-indonesia

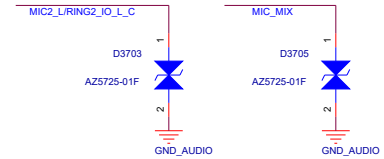
HP Detect



HP & MIC Connector



EXTERNAL MICROPHONE



Project Name: ALC285+SMARTAMP		Rev: R1.2
Title : AUD_EXT Jack		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 37 of 103	

EC 5125

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPG[0,1,6]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

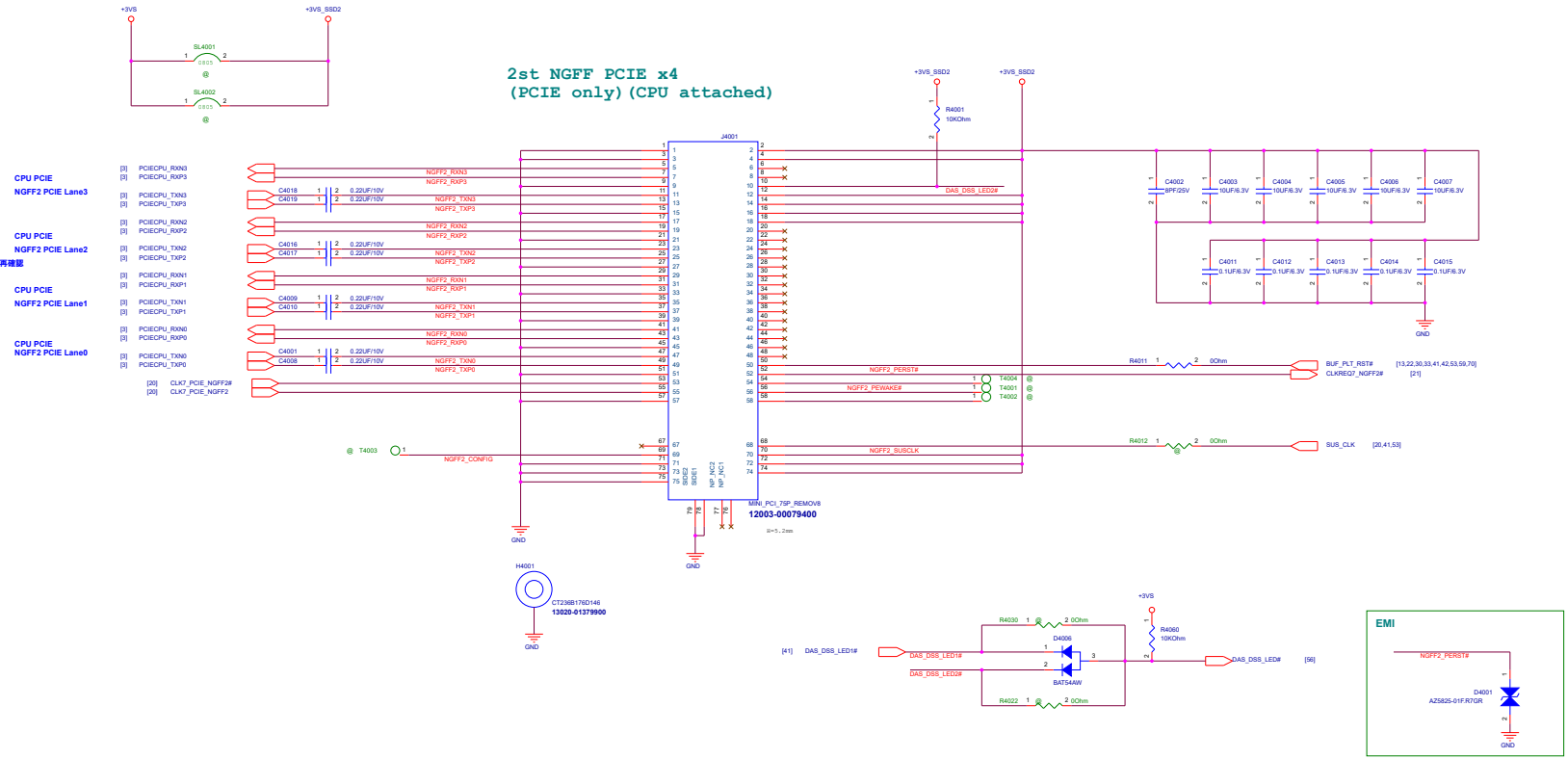
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8225VG-128/CX	06037-00260300
IT5125VG-128/CX	06037-00370000
IT5125VG-192/CX	06037-00370200

Power
R1.0-29
N key
20181202 add for power
PU/PD
for load code
GPD2 pull down for EC mirror
Support Slave CHG (Prevent from leakage)
0506 need to check with EC RD
Battery
Thermal sensor
For EMI
R1.0-34
IT5125VG-192/CX
2018/06/28 by James
須改為 1.8V
closed to pin A1
Modified for rising time by TG 20180731
N501
<Core Design>

ASUSTeK COMPUTER
Title : CR_KBC_IT8521
Engineer: EE
Size C | Project Name GX502GX | Rev R1.2
Date: Wednesday, March 17, 2021 | Sheet 30 of 103



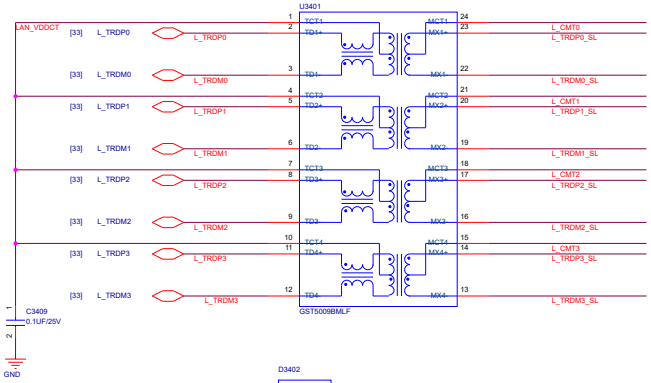
Pin#	Assignment	Description
1	GND	Return current path
3	GND	Return current path
5	PETn3	PCIe TX
7	PETp3	PCIe TX
9	GND	Return current path
11	PERn3	PCIe Rx
13	PERp3	PCIe Rx
15	GND	Return current path
17	PETn2	PCIe TX
19	PETp2	PCIe TX
21	GND	Return current path
23	PERn2	PCIe Rx
25	PERp2	PCIe Rx
27	GND	Return current path
29	PETn1	PCIe TX
31	PETp1	PCIe TX
33	GND	Return current path
35	PERn1	PCIe Rx
37	PERp1	PCIe Rx
39	GND	Return current path
41	PETn0	PCIe TX
43	PETp0	PCIe TX
45	GND	Return current path
47	PERn0	PCIe Rx
49	PERp0	PCIe Rx
51	GND	Return current path
53	REFCLKN	PCIe Reference Clock
55	REFCLKP	PCIe Reference Clock
57	GND	Return current path
67	N/C	N/C
69	PEDET	N/C
71	GND	Return current path
73	GND	Return current path
75	GND	Return current path

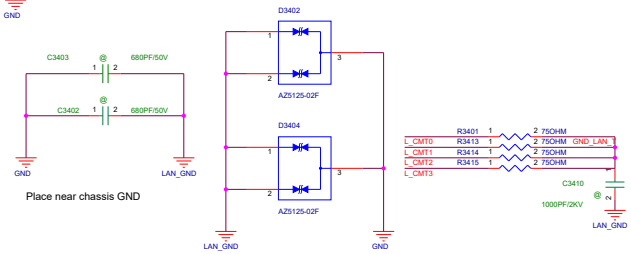
Pin#	Assignment	Description
2	3.3V	3.3V source
4	3.3V	3.3V source
6	N/C	N/C
8	N/C	N/C
10	LED1#[1]	Device Active Signal (Refer to [Table 11])
12	3.3V	3.3V source
14	3.3V	3.3V source
16	3.3V	3.3V source
18	3.3V	3.3V source
20	N/C	N/C
22	N/C	N/C
24	N/C	N/C
26	N/C	N/C
28	N/C	N/C
30	N/C	N/C
32	N/C	N/C
34	N/C	N/C
36	N/C	N/C
38	N/C	N/C
40	N/C	N/C
42	N/C	N/C
44	N/C	N/C
46	N/C	N/C
48	N/C	N/C
50	PERST#	PCIe Reset
52	CLKREQ#	PCIe Device Clock Request
54	PEWake#	N/C
56	Reserved for MFG_Data	N/C
58	Reserved for MFG_CLOCK	N/C
68	SUSCLK	N/C
70	3.3V	3.3V source
72	3.3V	3.3V source
74	3.3V	3.3V source

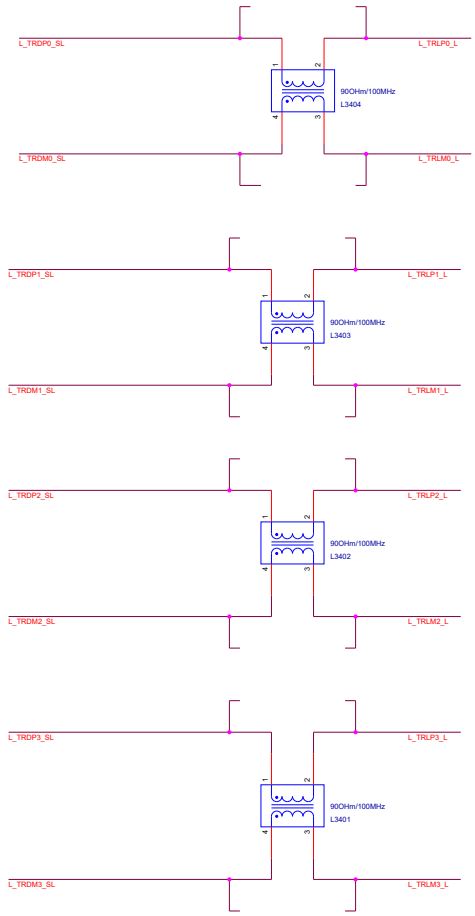
ASUS	Project Name: GX502GX	Rev: R1.2
Title :	NGFF_SSD_PCIE_CON	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 40 of 103	

20200526 modify

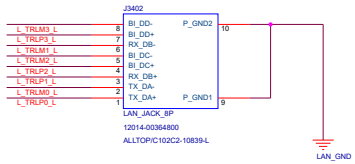
Main Board

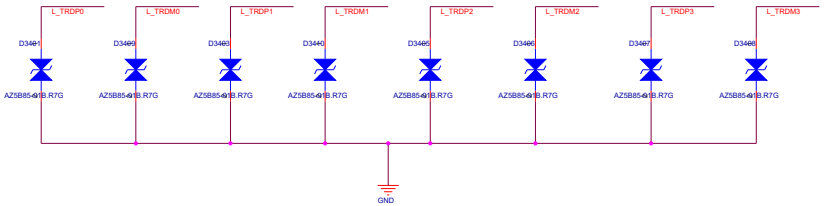






LAN Connector





D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

ASUS	Project Name: GX502GX		Rev: R1.2
Title : LAN_RJ45_CON			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 34 of 103		

for GX703

IT8237

Nkey_Power

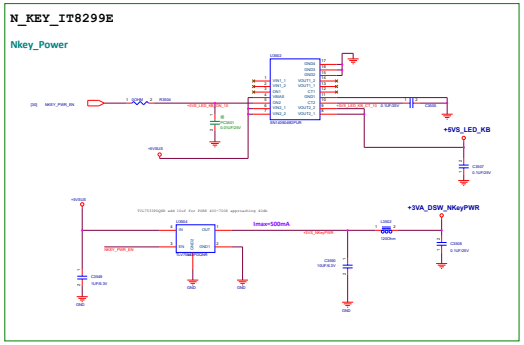
For EC Reset N_key

For IT8237 Debug

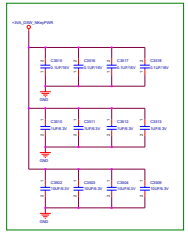
Keyboard Function Key

N_KEY_IT8299E

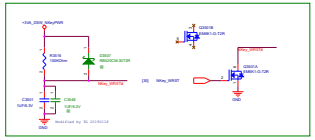
Nkey_Power



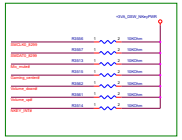
Nkey_Power_Cap



For EC Reset N_key

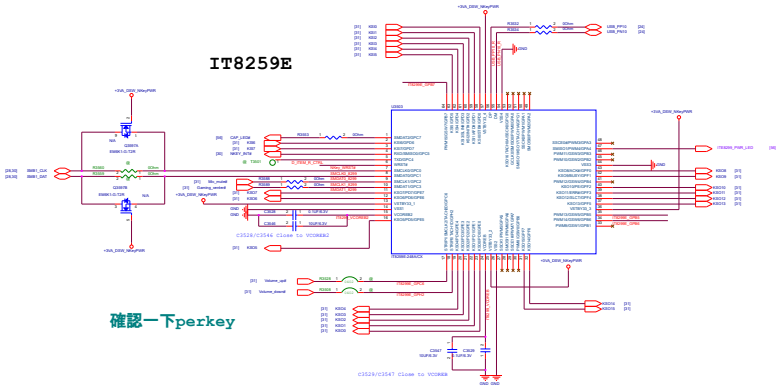


Pull up

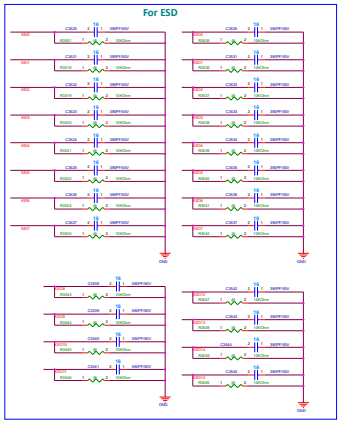


for GX703,GU603

IT8259E



For ESD

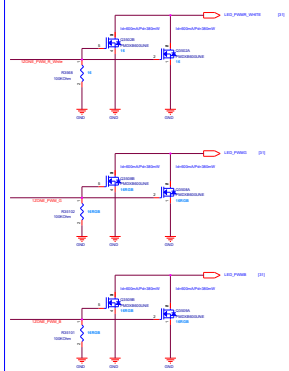


KB RGB Per Key LED(GX703)

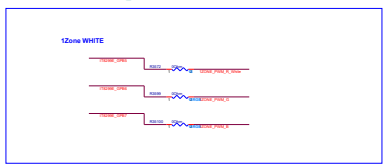
PerKey Signal(GX703)

KB WHITE LED(GU603)

** Add PerKey Use@070219A

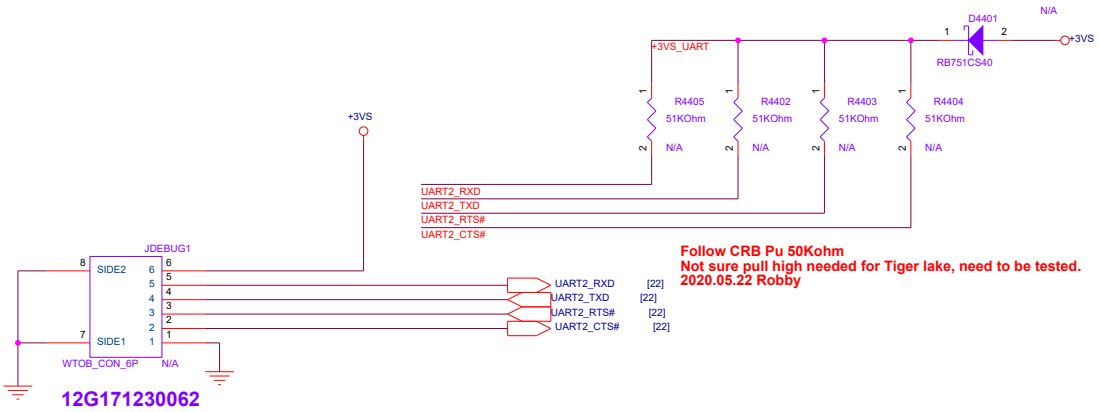


KB RGB co-layout



Title :	LAN *****		
Engineer:	EE		
Size	Project Name		Rev
Custom	GX502GX		R0.2
Date: Wednesday, March 11, 2020	Sheet	36 of 58	

UART Debug Port



Follow CRB Pu 50Kohm
Not sure pull high needed for Tiger lake, need to be tested.
2020.05.22 Robby

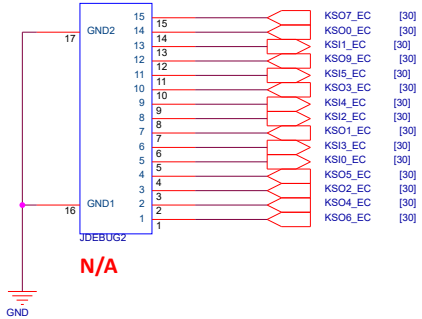
12G171230062

2017/11/10

Flash BIOS

12018-00390900

FPC_CON_15P



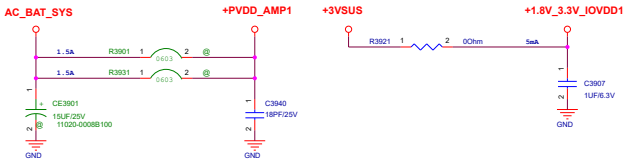
N/A

www.teknisi-indonesia.com

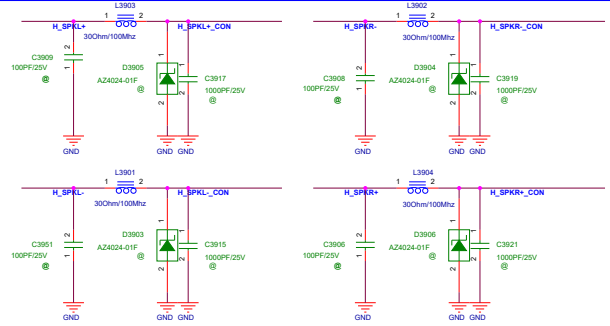
<Core Design>

ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: EE	
Size: B	Project Name: GX502GX	Rev: R1.2
Date: Wednesday, March 17, 2021	Sheet 44 of 103	

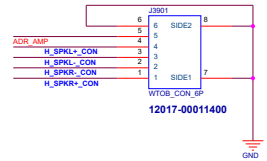
Power



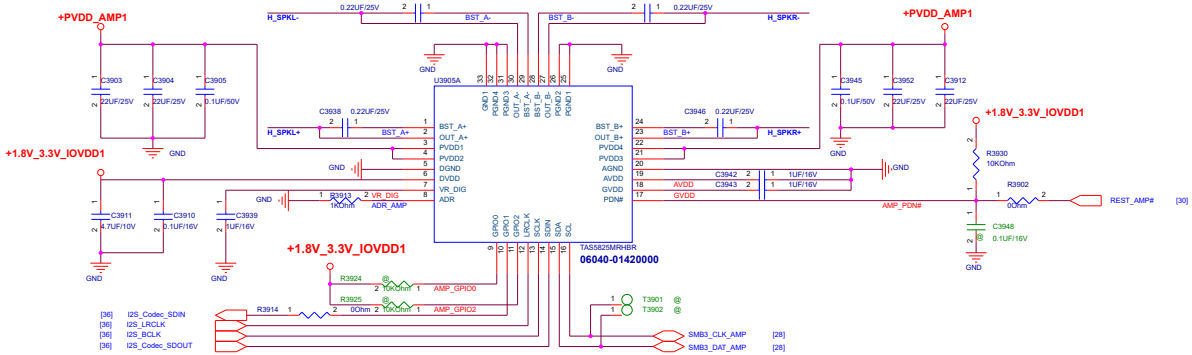
EMI

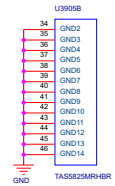


Main Speaker Connector



Main Speaker





I2C Address Table

	ADR_AMP(SPK)	Address 8bit
Main	Open	0x9A
Second	Short	0x98

Power

EMI

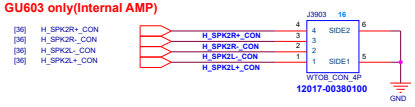
GX703 mount (External AMP)
GU603 unmount (Internal AMP)

HF Speaker Connector

GX703 only(External AMP)

HF Speaker Connector

GU603 only(Internal AMP)



Tweeter SPK (GX703 only)

I2C Address Table

	ADR_AMP2	Address 8bit
Main	15K	0x9E

ASUS	Project Name: ALC285+SMARTAMP		Rev: R1.2
Title : AUD_INT SPK			
Size: C	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 39 of 103		

Main Board

HDMI Active-Level Shift

Modify (20200604)

to GPU

From GPU

Q4801只用07005-00660200與07005-00950000

06106-00390100

SN75DP159RSBT

HDMI PWR_+5VS_HDMI

Remove SL4802 (20180927)

HDMI Conn.

GX703	12022-00137600
GU603	12022-00135300

HDMI EMI

Note:

The choke we use in the end is 09G092090400

HDMI LDO 1.1VS

Imax = 0.35A

Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow

HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: - 2 dB de-emphasis level
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved

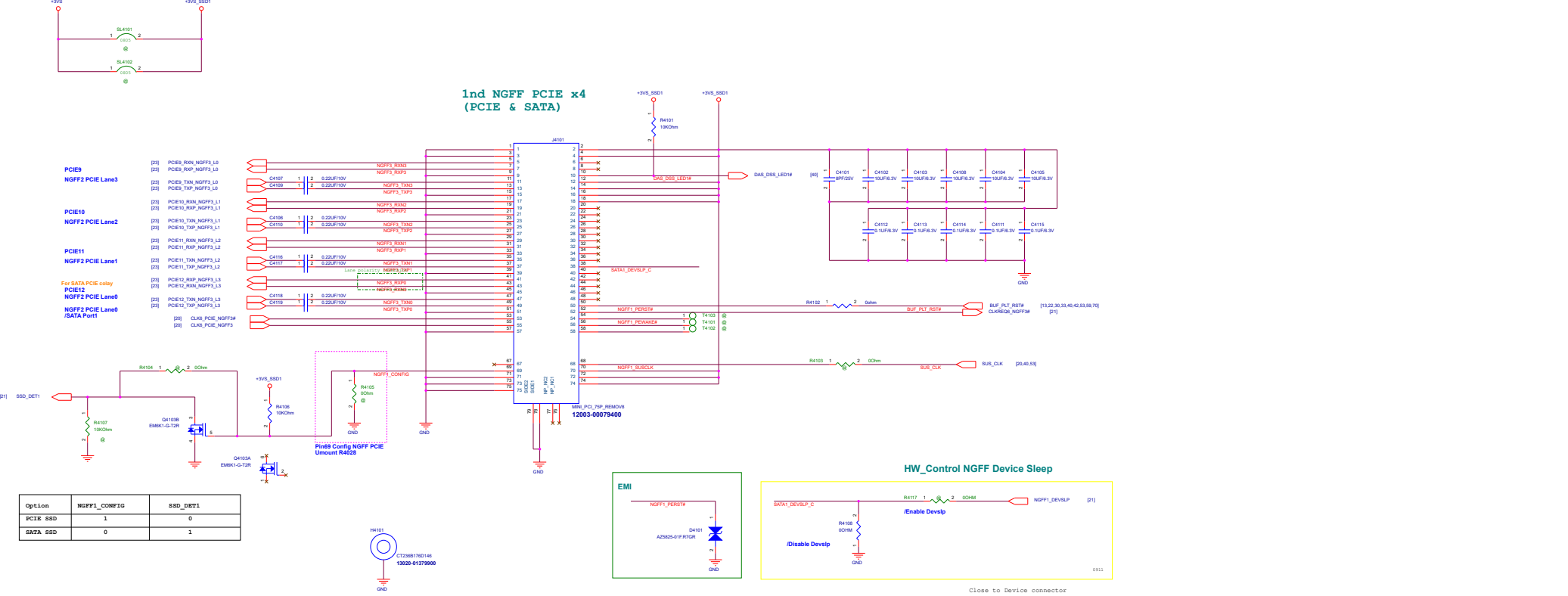
I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode

Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

[0912] Add C4813,C4819 Vendor suggest(power noise)

[0912] Add C4823,C4824 Vendor suggest(power noise)

Project Name	Design IP		Rev 0.1B
Title :	HDMI ReTimer_Revision History_R0.1B		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 48 of 103		



Option	NGFF1_CONFIG	SSD_DET1
PCIE SSD	1	0
SATA SSD	0	1

GX703GU503

Title : NGFF_SSD_CPU

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
Custom	GX703_GU603	R1.2

Date: Wednesday, March 17, 2021 Sheet 41 of 103

Power_3.3V

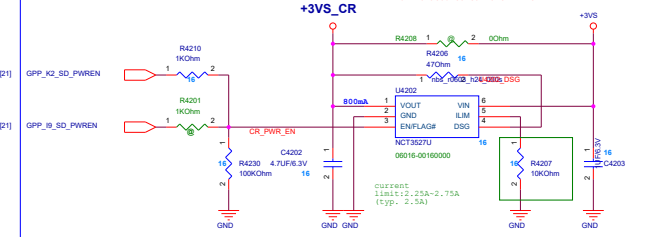
for RTD3
for layout placement

UHS-II consuption
+3VS_CR : 238.4mA(IC)+800mA(Card)=1.1A

Current Limit vs. R_{ILIM} Values

R_{ILIM} (Ω)	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
6.98k	2700	3000	3300
7.68k	2430	2700	2970
8.25k	2250	2500	2750
9.53k	1980	2200	2420
10.5k	1800	2000	2200
11.5k	1620	1800	1980
14.3k	1350	1500	1650
17.4k	1080	1200	1320
21k	900	1000	1100

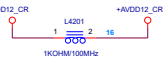
R4207 related to current limit



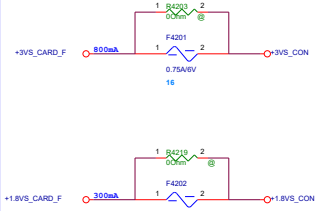
Power_3.3V

RTD3	Support	No Support
R4202	Unmount	Mount
R4204	Mount	Unmount

Power_1.2V

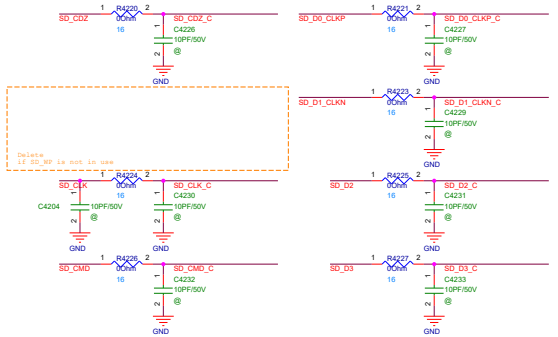


Safety

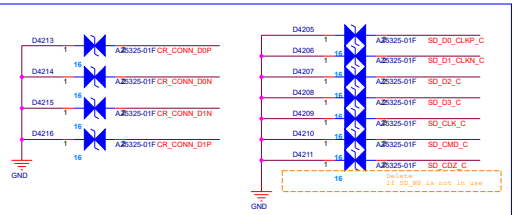


EMI

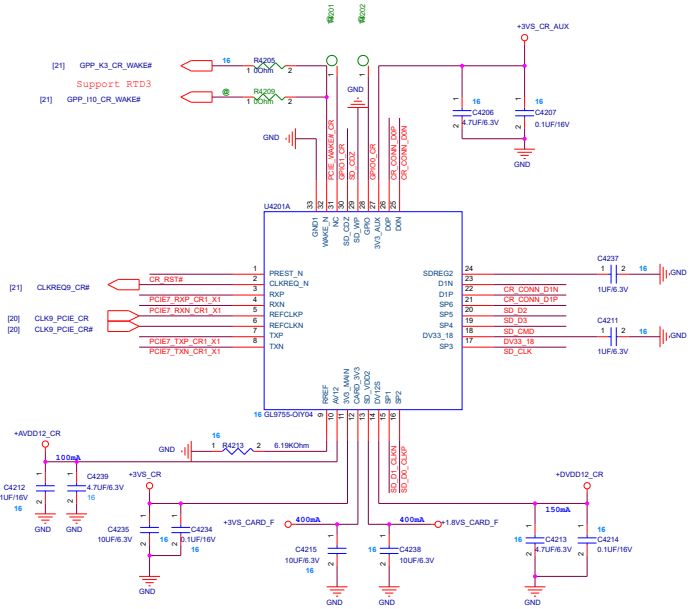
close to connector



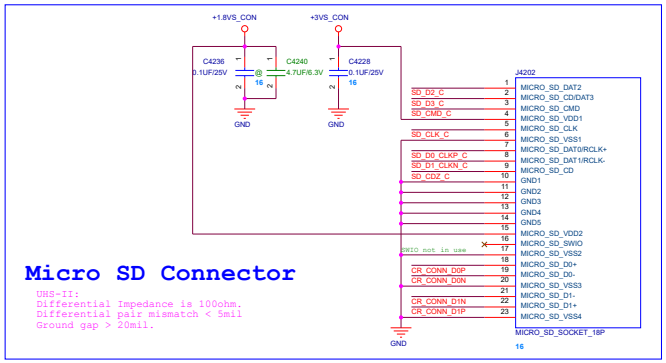
ESD



SD_WP if not in use
please connect to GND directly

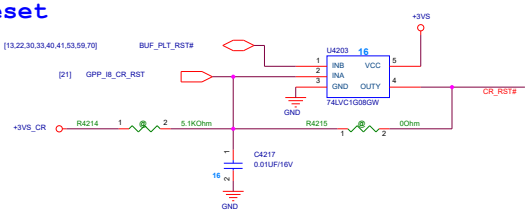


Micro SD Connector

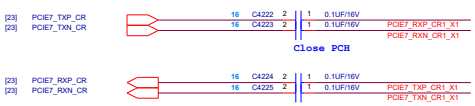


UHS-II:
Differential Impedance is 100ohm.
Differential pair mismatch < 5mil
Ground gap > 20mil.

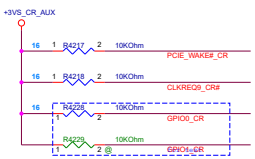
Reset

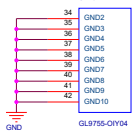


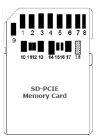
PCIE



Pull UP







PCIe/NVMe Interface is assigned to pads on the second row as well as sharing some of the pads in the first row.

Pin #	Name	Type	Description
1	PERST#	Input signal (active low)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
4	VDD1	Supply voltage	2.7V to 3.6V
7	REFCLK+	Differential Signaling. Input	Clock Input
8	REFCLK-	Differential Signaling. Input	Clock Input
9	CLKREQ#	I/O (active low, open drain)	Reference clock request signal. Also used by L1 PM substates
10	VSS3	Ground	
11	PCIe TX+	Differential Signaling	Card Input
12	PCIe TX-	Differential Signaling	Card Input
13	VSS4	Ground	
14	VDD2	Supply Voltage 2	1.70V to 1.95V
15	PCIe RX-	Differential Signaling	Card Output
16	PCIe RX+	Differential Signaling	Card Output
17	VSS5	Ground	
18*	VDD3	Supply Voltage 3	1.14v to 1.30v

(*) reserved for future optional VDD3 power

ASUS	Project Name	GX550L	Rev R1.4
Title :	CR_GL9755		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: TG_Wei	
Date: Wednesday, March 17, 2021	Sheet 42 of 103		

Thermal Sensor : SN170027

power rail : 3.3V

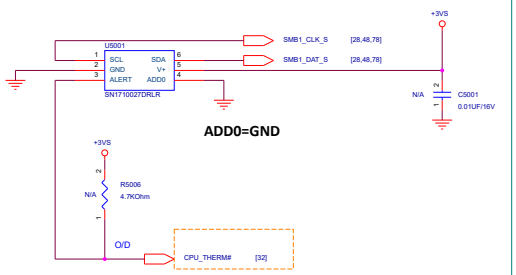
SMBUS1 to EC

Main Board

ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

Pin function Supply voltage.: 1.62 V to 3.6 V

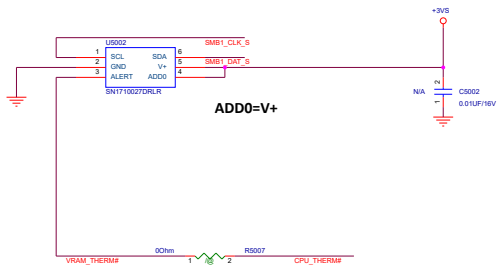
CPU



Near CPU

SMBUS addr=10010000 (90)

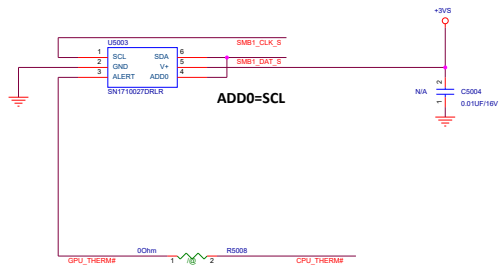
VRAM



Near VRAM

SMBUS addr=10010001 (92)

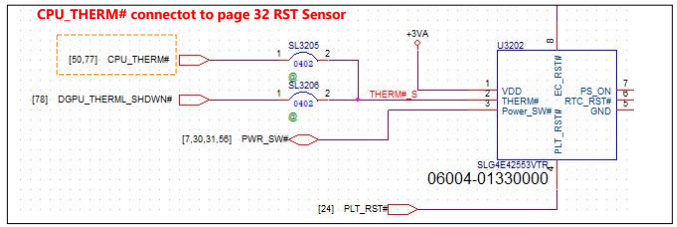
GPU



Near GPU

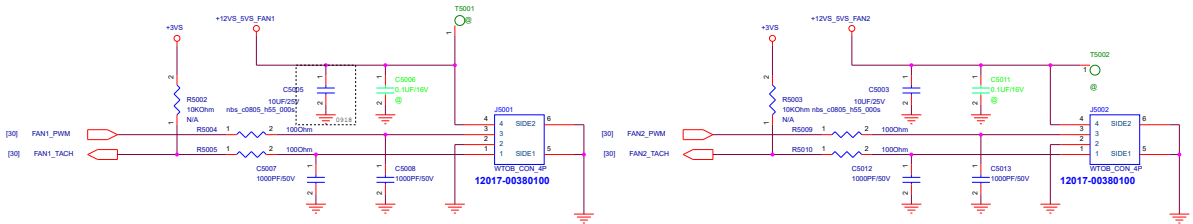
SMBUS addr=1001011 (96)

example



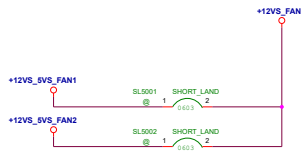
CPU&GPU FAN

Note : connector and power are by project design



ADD0: Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL



<Variant Name>

Title : Thermal Sensor

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size: Custom

Project Name: thermal sensor & fan

Rev: R1.0

Date: Wednesday, March 17, 2021

Sheet 50 of 103

Project Name

GX502GX

Rev

R1.2

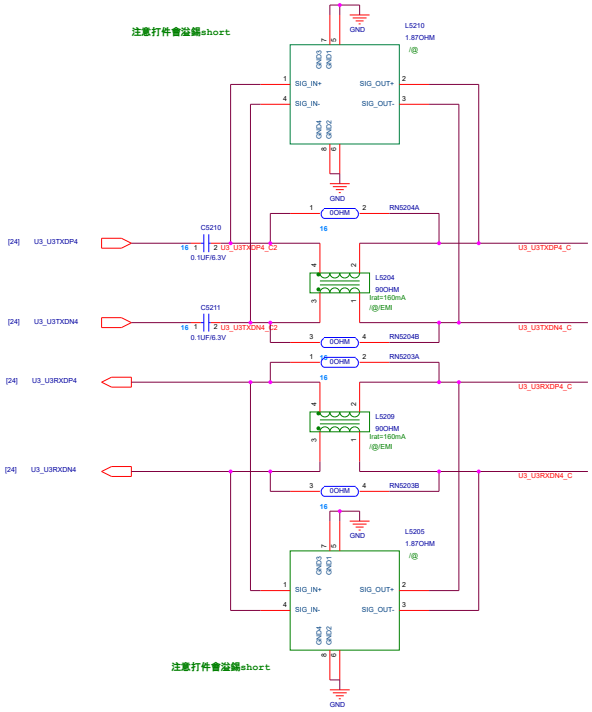
Title : CB_CON

Size	Dept.:	Engineer:
A	ASUSTeK COMPUTER	EE

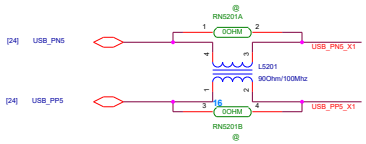
Date: Wednesday, March 17, 2021

TYPE-C USB3.1

USB3.0 EMI-Protection



[24] U3_U3TXDP4
[24] U3_U3TXDN4
[24] U3_U3RXDP4
[24] U3_U3RXDN4

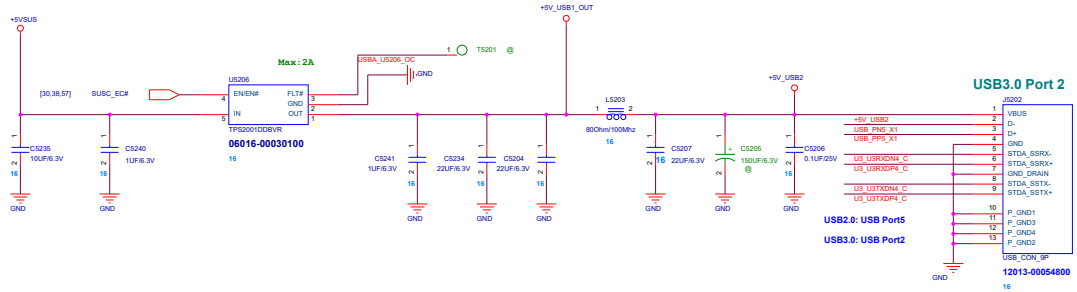


[24] USB_PN5
[24] USB_PP5
USB_PN5_X1
USB_PP5_X1

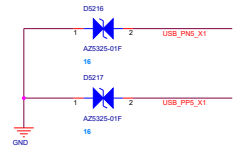
5.PIN DEFINE TABLE:

PIN NO.	1	2	3	4
SIGNAL NAME	VBUS	D-	D+	GND

PIN NO.	5	6	7	8	9
SIGNAL NAME	StdA_SSRX-	StdA_SSRX+	GND-DRAIN	StdA_SSTX-	StdA_SSTX+



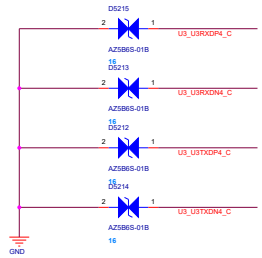
USB2.0 ESD-Protection



For EMI, Lloyd 2020/5/28

USB3.0 ESD-Protection

1st Source: P/N:07024-01360000 ESD PROTECTION AZ5B6S-01B



<Core Design>

ASUSTeK COMPUTER	Title : USB Charger	
	Engineer: EE	
Size: Custom	Project Name: GX502GX	Rev: R1.2
Date: Wednesday, March 17, 2021	Sheet 52 of 103	

*** POWER

** [P.88] +3VS → +3VS
** [P.87] +3VSUS → +3VSUS
** [P.87]
** [P.84] +1.8VSUS → +1.8VSUS
** [P.88] +5VS → +5VS
** [P.87] +5VSUS → +5VSUS
** [P.87] +12VS → +12VS
+3VA_EC → +3VA_EC

*** SINGAL

** PCH Control

[21] ACZ_BCLK_AUD → ACZ_BCLK_AUD
[21] ACZ_SYNC_AUD → ACZ_SYNC_AUD
[21] ACZ_SDIN0_AUD → ACZ_SDIN0_AUD
[21] ACZ_SDOUT_AUD → ACZ_SDOUT_AUD
[21,37] ACZ_RST#_AUD → ACZ_RST#_AUD

** EC Control

[30] AMP_SLEEP# → AMP_SLEEP#
[30] OP_SD# → OP_SD#

** Jack Control

[37] EAPD# → EAPD#
[37] TOU_CON_L → TOU_CON_L

** To EXT. Amp.

[39] I2S_Codec_SDIN → I2S_Codec_SDIN
[39] I2S_Codec_SDOUT → I2S_Codec_SDOUT
[39] I2S_BCLK → I2S_BCLK
[39] I2S_LRCLK → I2S_LRCLK

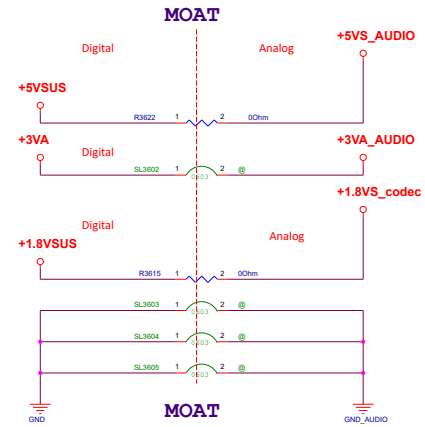
** Headset Connection

[37] LINE1_R → LINE1_R
[37] LINE1_L → LINE1_L
[37] MIC2_R_SLEEVE → MIC2_R_SLEEVE
[37] MIC2_L_RING2 → MIC2_L_RING2
[37] MIC2_VREFO_R → MIC2_VREFO_R
[37] MIC2_VREFO_L → MIC2_VREFO_L
[37] HPOUT_L → HPOUT_L
[37] HPOUT_R → HPOUT_R

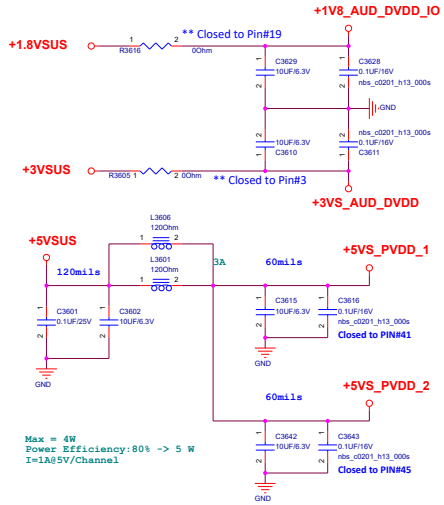
** Tweeter AMP CONN Connection

[39] H_SPK2L+_CON → H_SPK2L+_CON
[39] H_SPK2L-_CON → H_SPK2L-_CON
[39] H_SPK2R-_CON → H_SPK2R-_CON
[39] H_SPK2R+_CON → H_SPK2R+_CON

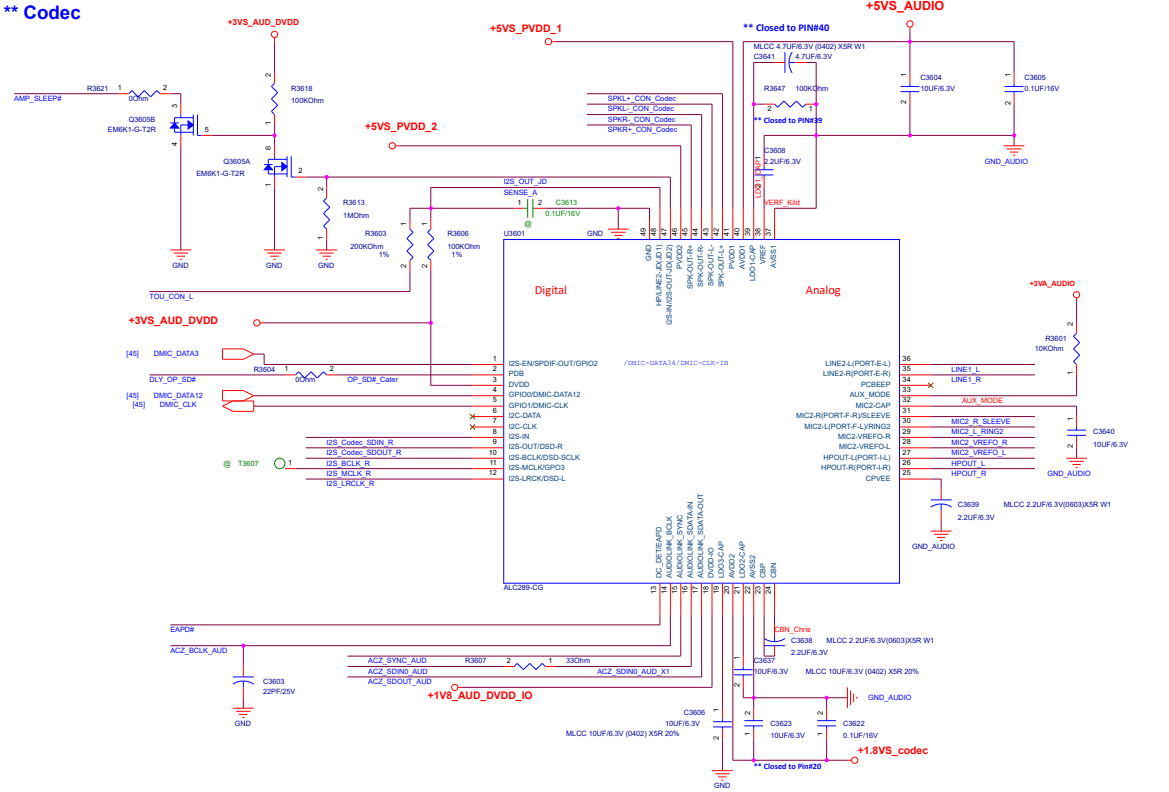
** PWR DISTRIBUTION (ANALOG)



** PWR DISTRIBUTION (DIGITAL)

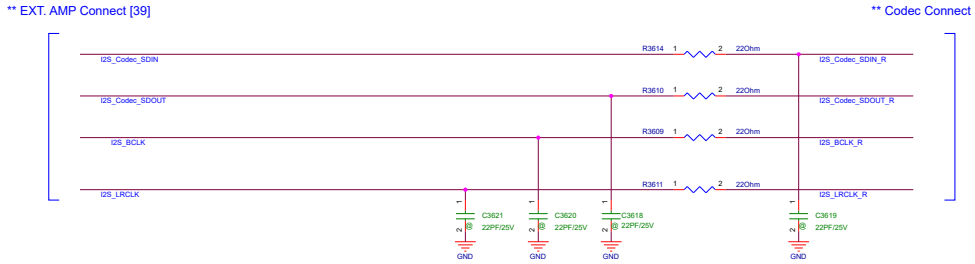


** Codec

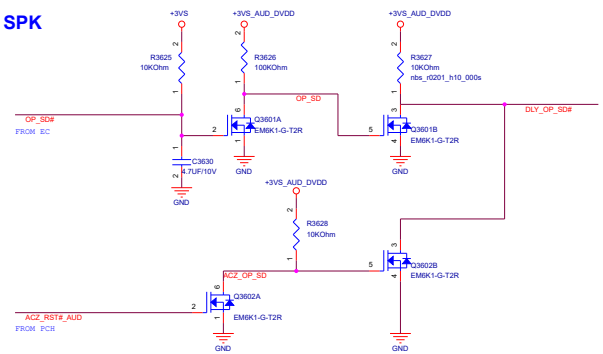


** EXT. AMP Connection

teknisi-indonesia

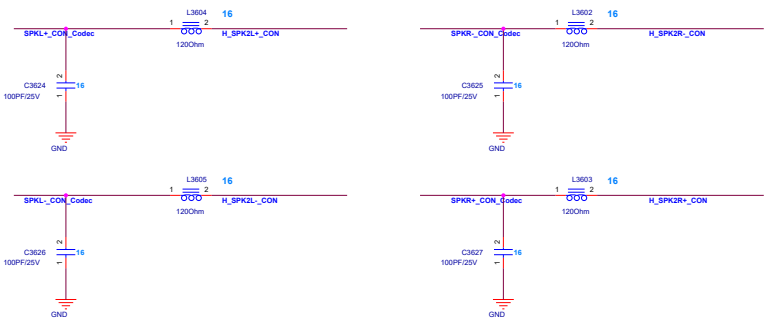


** Codec Internal SPK MUTE CONTROL

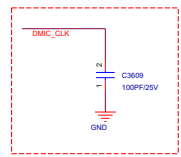


** Tweeter AMP CONN. (GU603)

GX703 unmount (External AMP)
GU603 mount (Internal AMP)



EMI

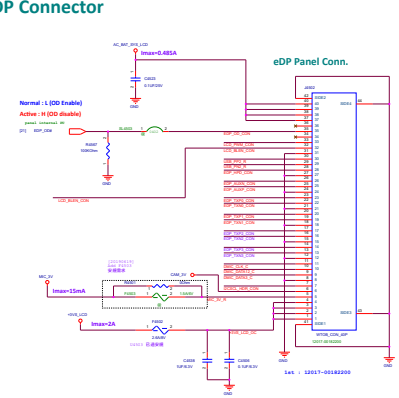


<Core Design>

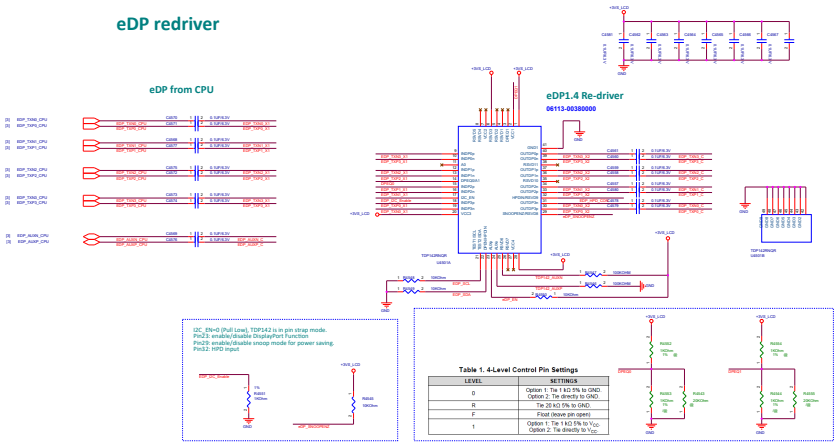
ASUS	Project Name: ALC285+SMARTAMP	Rev: R1.3
Title :	AUD-ALC285	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Date: Wednesday, March 17, 2021	Sheet 36 of 103	

Panel BL Power

eDP Connector

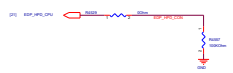


eDP redriver

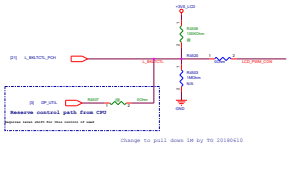


LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 kΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.

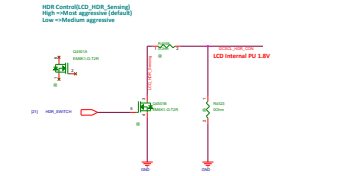
eDP_HPD (CPU)



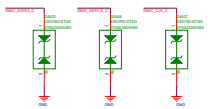
eDP_BL PWM



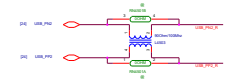
Pin34 : HDR Panel or DDS I2C SCL



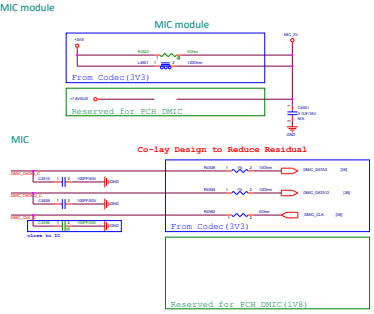
For ESD(MIC)



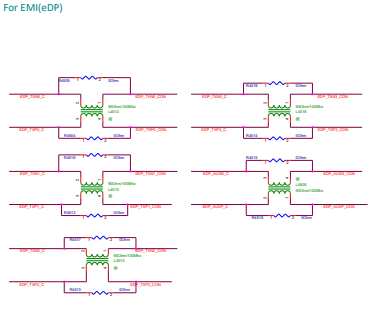
Camera



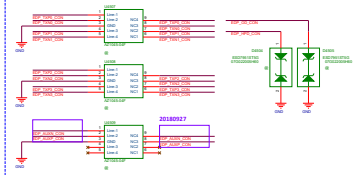
MIC module



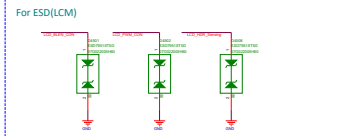
For EMI(eDP)

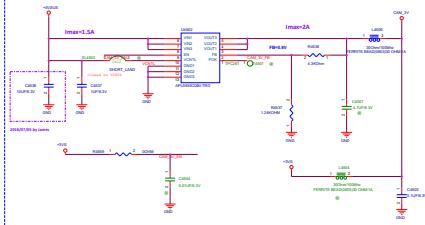


For ESD(eDP)

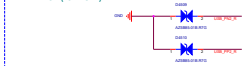


For ESD(LCM)



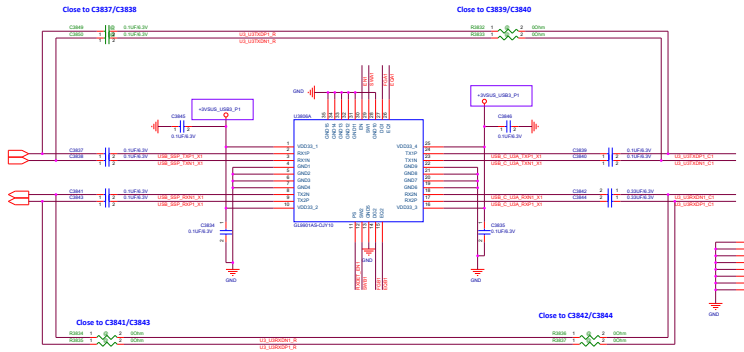


ESD(for LCM)

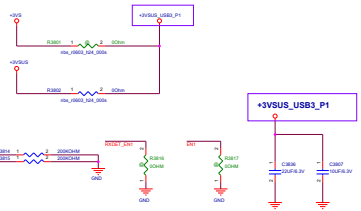


Title :	CRT_eDP		
Engineer:	EE		
Size	Project Name	Rev	
Custom	GX502GX	R1.2	
Date: Wednesday, March 07, 2018	Sheet 45 of 102		

[Bypass Path]

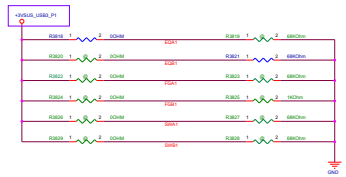


Imax = 0.2A



< Channel / Power saving mode setting for Genesys GL9901AS >

Setting	Channel Enable [EN]	Power saving mode [RXDET_EN]
0 : 0 Ω to GND	Disable	Disable
1 : 0 Ω to VDD	Enable(Default)	Enable(Default)
Note	Channel Enable / Power saving mode setting With internal pull-up.	



< Fine tune table for Genesys (One port Gen2) >

< EQ table for Genesys GL9901AS >

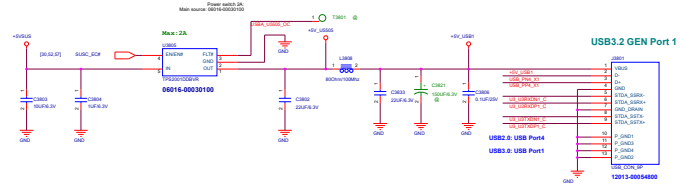
EQ	EQ @2.5GHz(dB)	EQ @5GHz(dB)
0 : 0 Ω to GND	6.3	10.1
R : Tie 68K to GND	2.2	4.4
F : Leave Open	4.1	7.1
1 : 0 Ω to VDD	7.6	11.6

<DC Gain table for Genesys GL9901AS >

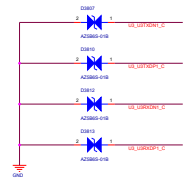
DGx Setting	Gain Level(dB)
0 : 0 Ω to GND	-2.0
R : Tie 68K to GND	-0.5
F : Leave Open	+0.5
1 : 0 Ω to VDD	+2.0

< SW table for Genesys GL9901AS >

SWx Setting	Output Swing Level (mV)
0 : 0 Ω to GND	800
R : Tie 68K to GND	1200
F : Leave Open	1000
1 : 0 Ω to VDD	1100



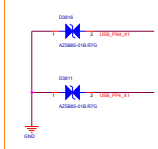
USB3.0 ESD-Protection



ESD PROTECTION

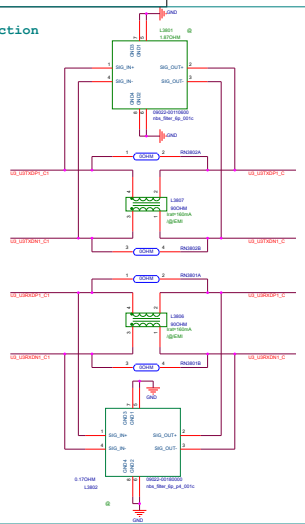
1st Source: P/N:07024-01360000 ESD PROTECTION AZ5865-01B

USB2.0 ESD-Protection



For EMI, Eason 2018/7/25

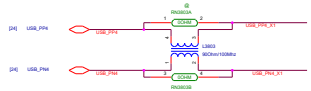
USB3.0 EMI-Protection



R1.5

USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

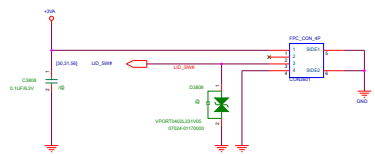
From PCH USB2.0 Port



Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C3809&C3810 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

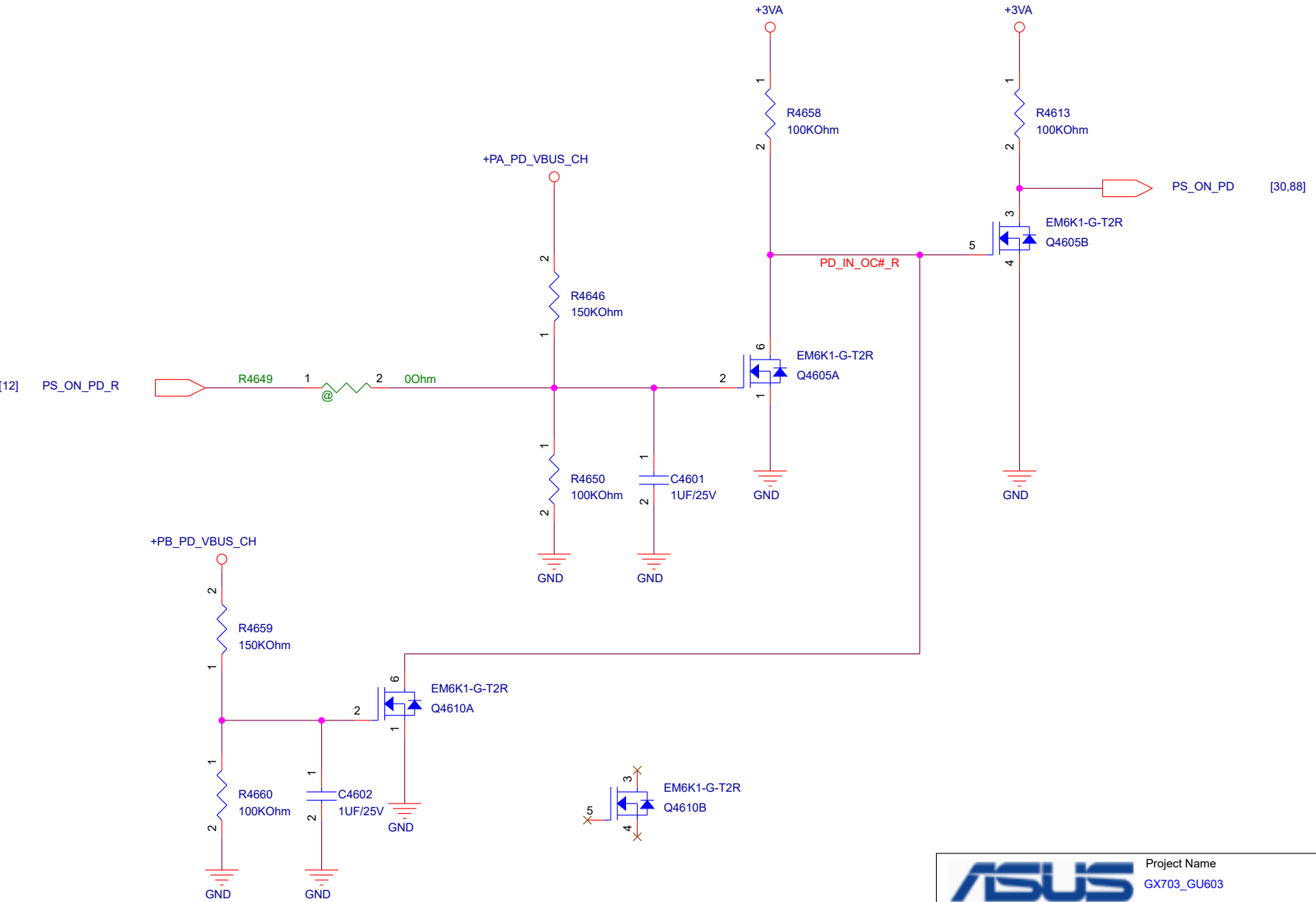
temp_M08_000010層名順序是 : TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

HALL SENSOR CONN (GU603&GX703)



current: 1mA

PD SINK connect



ASUS	Project Name: GX703_GU603	Rev: 1.0
Title : PD_TPS65993AC		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Design IP
Date: Wednesday, March 17, 2021	Sheet 46 of 103	

Title <Title>		
Size A	Document Number <Doc>	Rev R1.2
Date: Wednesday, March 17, 2021	Sheet 54 of 103	

<Core Design>

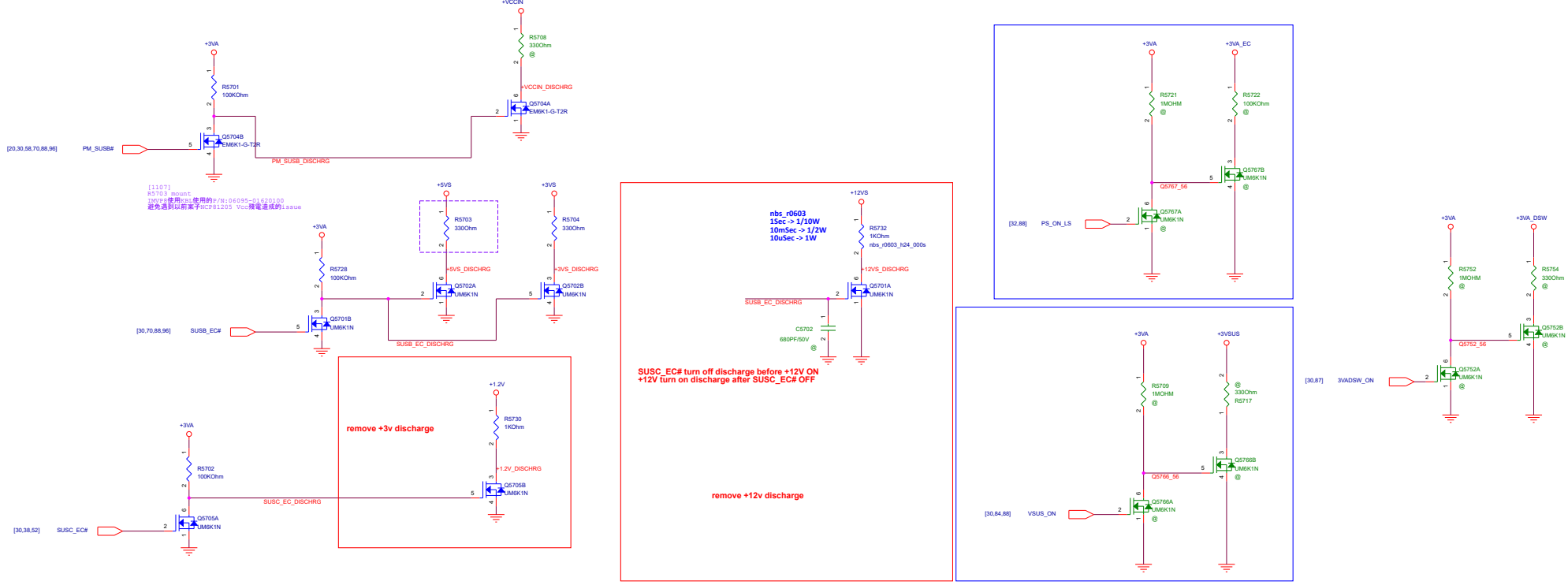
Title : IO Con. to MB

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.2

Date:	Wednesday, March 17, 2021	Sheet	55	of	103



20191106 增加discharge schematic for C10, VCCIO unmount for reserve

0526 remove +12VS_VCCSTG_VCCPLL_OC discharge

<Core Design>

ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: EE	
Size: C	Project Name: GX502GX	Rev: R1.2
Date: Wednesday, March 17, 2021	Sheet 57 of 103	

MAIN		U4901 RFASWA585BTF0C		
ANT	Port	V1 GPP_B0	V2	V3
ANT_1	RF1	1		
ANT_2	RF2	0		

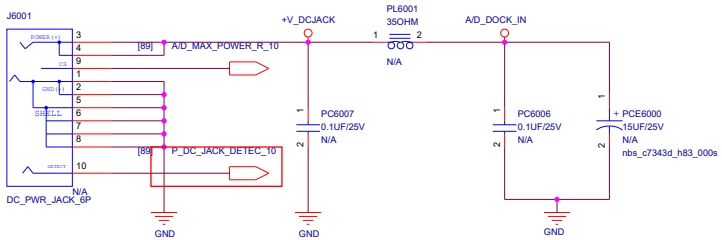
AUX		U4902 RFASWA585BTF0C		
ANT	Port	V1 GPP_B2	V2	V3
ANT_3	RF1	1		
ANT_4	RF2	0		

<Core Design>

ASUS	Project Name: GX502GX	Rev: R1.2
Title : ANT		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 17, 2021	Sheet 49 of 103	

DC-IN Connector

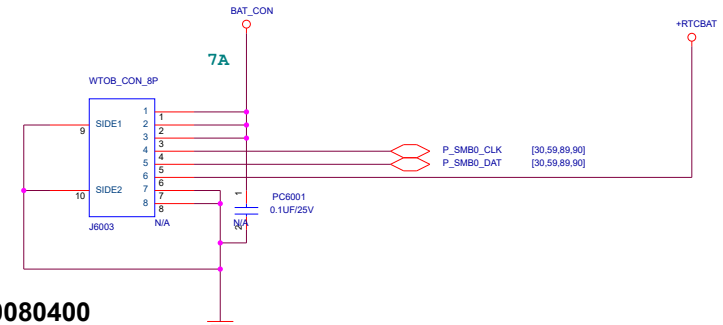
```
6 Phi 4 Pin DC_Jack +0.20ch --> GU603H
+2.10ch --> GX703H
```



12033-00020500

J6001	+0.20CH For GU603H	+2.10CH For GX703H
	12033-00020500	12033-00020400

Battery Connector



12017-00080400

Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

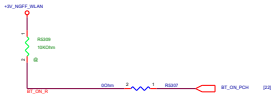
ASUS	Project Name: GX502GX		Rev: R1.2
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Wednesday, March 17, 2021	Sheet 60 of 103		

Control

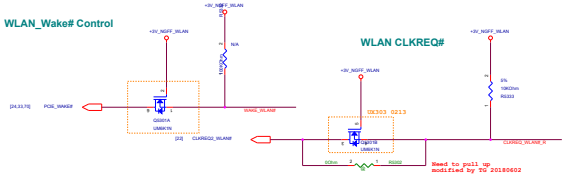
WLAN card Vendor recommend: (Intel/Realtek)
1. Module internal PU
2. Placeholder for protect unexpected issue

WLAN Ext_HW_Kill

BT Ext_HW_Kill



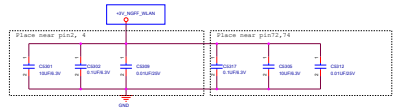
WLAN_Wake# Control



PU&PD

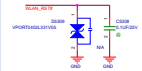
If Checklist show close to PCH
Please tell EE members, and add in PCH page

Bypass capacitor



For EMI

Reserve for power noise

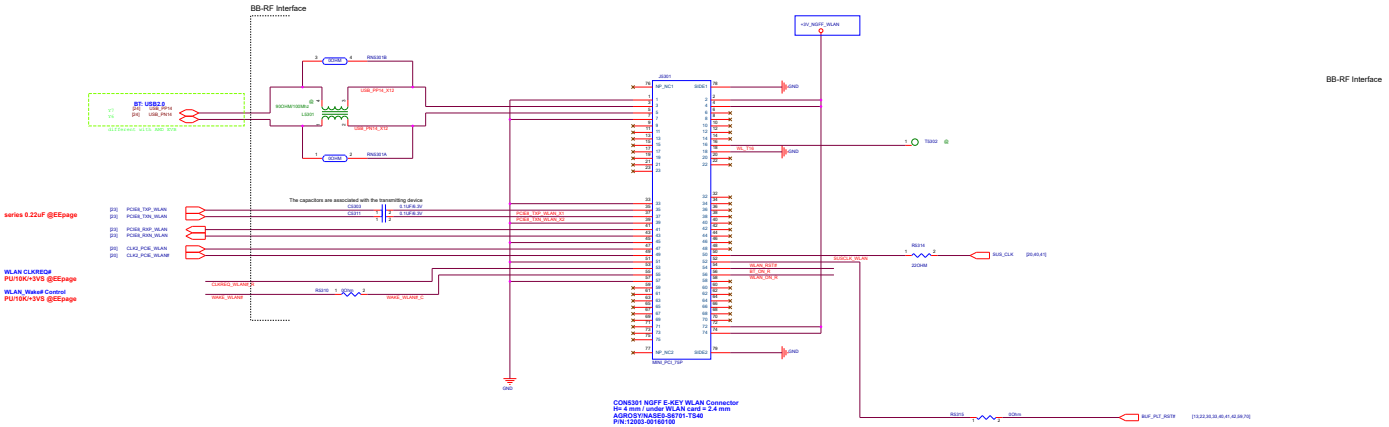


Power

WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)
Support ASUS Open Cloud Computing (AOConnect)

Others

Screw Hole



Max:210mA

+3VSUS_MUX_PB

close to U4706 VDD pin

+3VSUS

L4709 120Ohm

C4756 10UF/6.3V
C4754 0.1UF/10V
C4757 0.1UF/10V
C4758 0.1UF/10V
C4782 0.1UF/10V
C4735 0.1UF/10V
C4737 0.1UF/10V
C4738 0.1UF/10V
GND

Address 0xAE(W)

+3VSUS_MUX_PB

R4776 100KOhm
R4778 100KOhm
R4780 100KOhm
PB_A0
PB_A1
PB_A2
R4722 100KOhm
R4721 100KOhm
R4720 100KOhm
GND

[24] U3_U3RXDN3
[24] U3_U3RXDP3
C4716 0.1UF/6.3V
C4717 0.1UF/6.3V
PB_SSRXN
PB_SSRXP

[24] U3_U3TXDN3
[24] U3_U3TXDP3
C4718 0.1UF/6.3V
C4719 0.1UF/6.3V
PB_SSTXN
PB_SSTXP

[12,78] IFPE_DP_HPD
R4763 0Ohm

T4704 @
T4703 @
+3VSUS_MUX_PB

U4706B
GND19 GND18 GND17 GND16 GND15 GND14 GND13 GND12 GND11 GND10 GND9 GND8 GND7 GND6 GND5 GND4 GND3 GND2
PI3DPX1205AZLB
GND

+3VSUS_MUX_PB
R4792 10KOhm

U4706A
PI3DPX1205AZLB
AP_SSTXP AP_SSTXN VDD3.3_4 AP_HPD AP_SSRXN DCI_DAT

[12] PB_MUX_1205A_EN
[79] IFPE_DP1_TXP1
[79] IFPE_DP1_TXN1
[79] IFPE_DP1_TXP0
[79] IFPE_DP1_TXN0
[79] IFPE_DP1_TXN2
[79] IFPE_DP1_TXP2
[79] IFPE_DP1_TXN3
[79] IFPE_DP1_TXP3
R4790 0Ohm
C4706 0.1UF/6.3V
C4705 0.1UF/6.3V
C4702 0.1UF/6.3V
C4701 0.1UF/6.3V
C4704 0.1UF/6.3V
C4703 0.1UF/6.3V
C4708 0.1UF/6.3V
C4707 0.1UF/6.3V
PB_EN
PB_DP_TXP1
PB_DP_TXN1
PB_DP_TXP0
PB_DP_TXN0
PB_DP_TXN2
PB_DP_TXP2
PB_DP_TXN3
PB_DP_TXP3

EN AP_DP1P AP_DP1N VDDD3_5 AP_DP0P AP_DP0N VDDD3_6 AP_DP2N AP_DP2P VDDD3_7 AP_DP3N AP_DP3P GND1
CON_TX2P CON_TX2N A2 VDDD3_3 CON_RX2P CON_RX2N VDDD3_2 A1 CON_TX1N CON_TX1P VDDD3_1 A0

C4760 0.22UF/6.3V
C4759 0.22UF/6.3V
PB_CTX2P_C
PB_CTX2N_C
PB_A2
C4739 0.33UF/6.3V
C4741 0.33UF/6.3V
PB_CRX2P_C
PB_CRX2N_C
PB_A1
C4752 0.22UF/6.3V
C4753 0.22UF/6.3V
PB_CTX1N_C
PB_CTX1P_C
PB_A0
PB_CTX2P
PB_CTX2N
PB_CRX2P
PB_CRX2N
PB_CTX1N
PB_CTX1P
R4725 229kOhm
R4724 229kOhm
GND GND

+3VSUS_MUX_PB
R4753 100KOhm
R4754 100KOhm
GND

[79] IFPE_DP1_AUXP
[79] IFPE_DP1_AUXN
C4724 0.1UF/6.3V
C4725 0.1UF/6.3V
PB_AUXP
PB_AUXN

[12] MUX_I2C3_DAT
[12] MUX_I2C3_SCL
R4782 0Ohm
R4781 0Ohm

C4785 0.33UF/6.3V
C4786 0.33UF/6.3V
PB_CRX1N_C
PB_CRX1P_C
PB_CRX1N
PB_CRX1P
R4726 229kOhm
R4727 229kOhm
GND GND

ALT_PB_SBU1 [12]
ALT_PB_SBU2 [12]

R4729 4.7KOHM
R4723 4.7KOHM
+3VSUS
R4730 2MOHM
R4731 2MOHM
GND GND

TYPE-C Connector Port B

+5V_VBUS_PB

J4701
GND4 SSTXp2 SSTXn2 VBUS4 CC2 Dn2 Dp2 SBU2 VBUS3 SSRXn1 SSRXp1 GND2
GND1 SSTXp1 SSTXn1 VBUS1 CC1 Dp1 Dn1 SBU1 VBUS2 SSRXn2 SSRXp2 GND3
P_GND1 P_GND2 P_GND3 P_GND4 P_GND5 P_GND6
NP_NC1 NP_NC2
USB_CON_24P

PB_SSTXP2
PB_SSTXN2
PB_CC2
PB_USB3_C_U2_P_X1
PB_USB3_C_U2_N_X1
PB_SBU2
PB_SSRXN1
PB_SSRXP1
PB_SSTXP1
PB_SSTXN1
PB_CC1
PB_USB3_C_U2_P_X1
PB_USB3_C_U2_N_X1
PB_SBU1
PB_SSRXN2
PB_SSRXP2
[12] PB_CC2
[12] PB_SBU2
[12] PB_CC1
[12] PB_SBU1

12013-00171700

+PD_VBUS_PB
L4721 26OHM
FERRITE BEAD (0603) 26OHM/6A

+5V_VBUS_PB

20190702
VBUS capacitor , Close to Connector for VBUS1 to VBUS4

D4733 AZ4024-01F
C4721 0.01UF/50V
C4723 0.01UF/50V
C4720 0.01UF/50V
C4722 0.01UF/50V
GND

RN4705B 90Ohm L4711 RN4705A
PB_CTX2P PB_CTX2N PB_SSTXP2 PB_SSTXN2

RN4707A L4713 90Ohm RN4707B
PB_CTX1N PB_CTX1P PB_SSTXN1 PB_SSTXP1

RN4706A L4712 90Ohm RN4706B
PB_CRX2P PB_CRX2N PB_SSRXP2 PB_SSRXN2

RN4708B L4714 90Ohm RN4708A
PB_CRX1N PB_CRX1P PB_SSRXN1 PB_SSRXP1

[24] USB_PN3
[24] USB_PP3
RN4709A L4704 90Ohm/100Mhz RN4709B
PB_USB3_C_U2_N_X1
PB_USB3_C_U2_P_X1

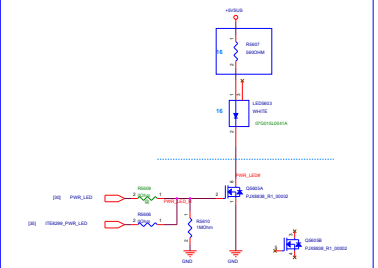
D4723 D4724 D4725 D4726 D4727 D4728 D4729 D4730 AZ5B6S-01B
PB_SSTXP2 PB_SSTXN2 PB_SSRXP2 PB_SSRXN2 PB_SSTXP1 PB_SSTXN1 PB_SSRXN1 PB_SSRXP1

D4719 D4720 D4721 D4722 D4731 D4732 AZ5325-01F
PB_USB3_C_U2_P_X1
PB_USB3_C_U2_N_X1
PB_CC1
PB_CC2
PB_SBU1
PB_SBU2
GND

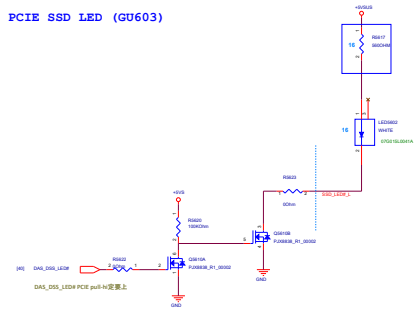
ASUS	Project Name: GX703_GU603		Rev: 1.0
Title :	USB3.1 TYPE-C+PI3DPX1205AZL		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Design IP
Date: Wednesday, March 17, 2021	Sheet: 47	of:	103

Main Board

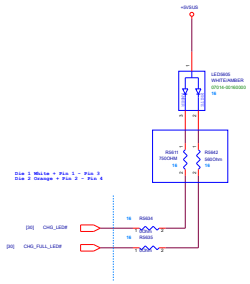
PWR LED (GU603)



PCIE SSD LED (GU603)



Charger LED (GU603)



for GX703 SUB BOARD(High Speed Signal)

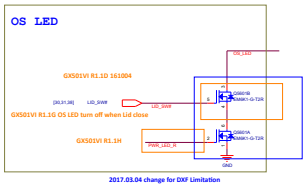
Connect to page 66

for GX703 SUB BOARD(Power)

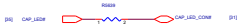
Connect to page 66

for GX703 indicator LED board

OS LED

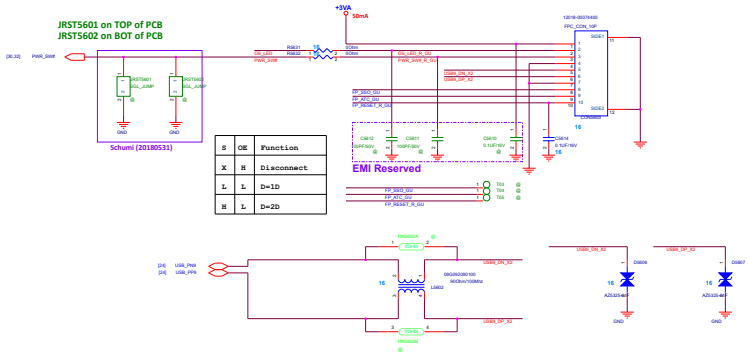


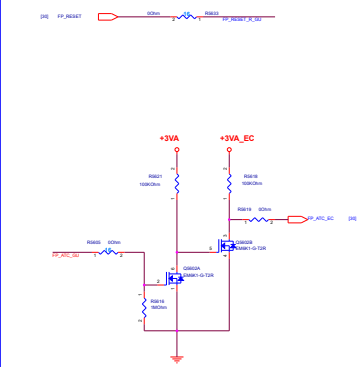
CAP LED

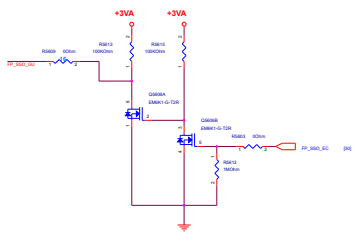


Power Key and FigerPrinter (GX703)

Power Key and FigerPrinter (GU603)







Wheel/LED for GX703

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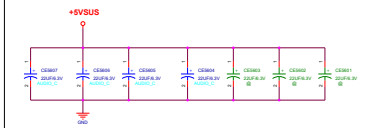
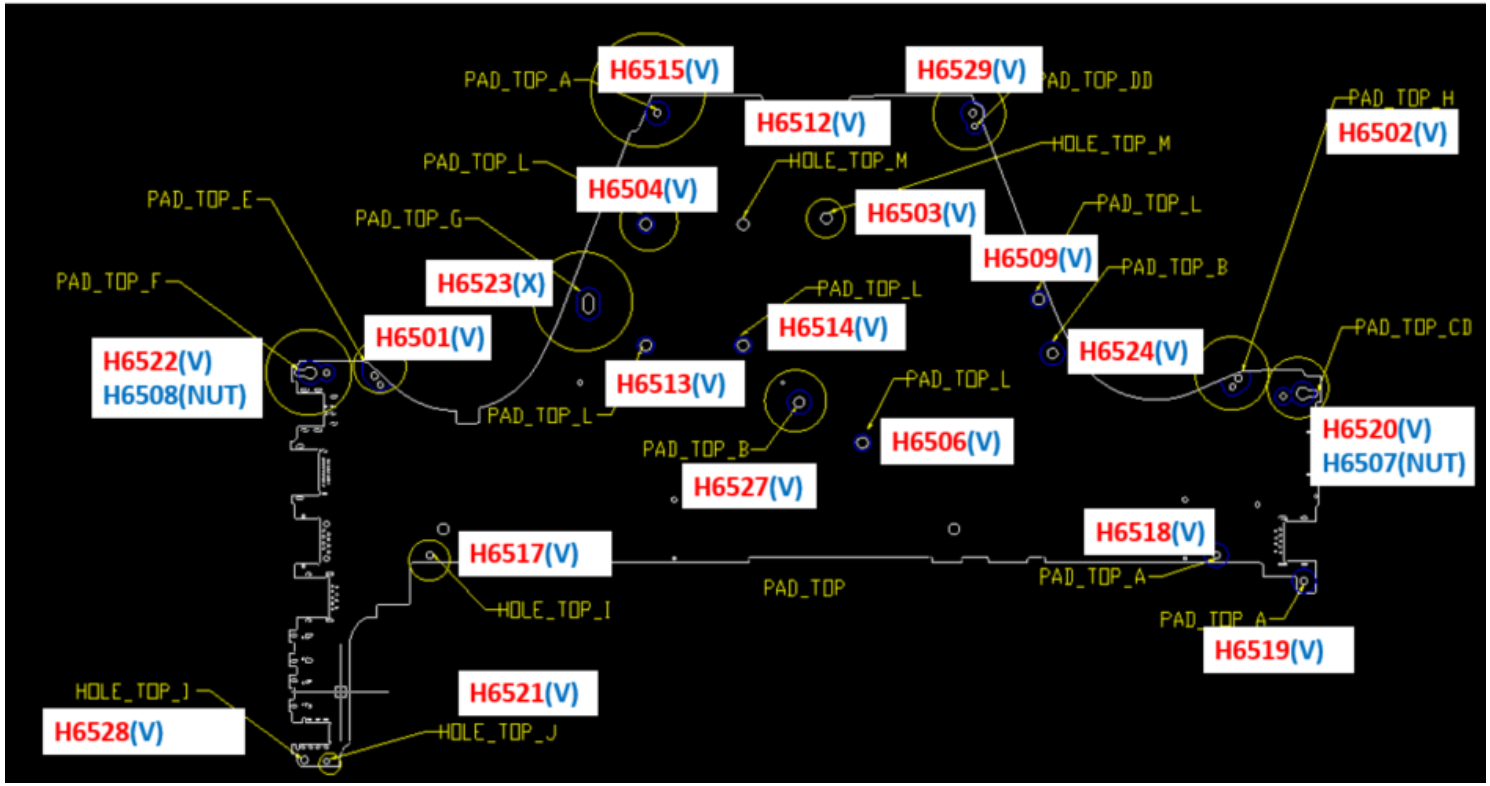
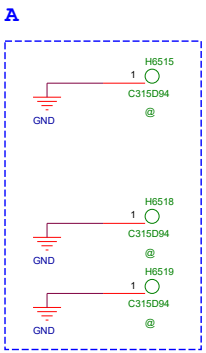
Caps for Acoustic noise

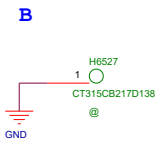


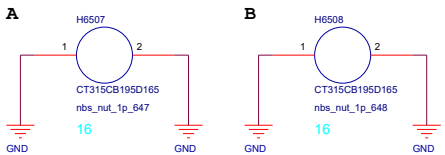
Title :	LED & LID
Engineer:	EE
Project Name	GX502GX
Rev	R1.2

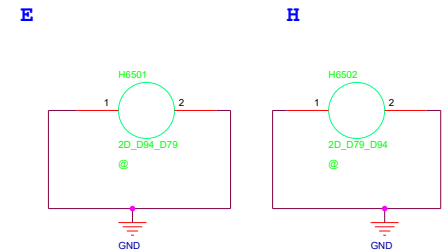


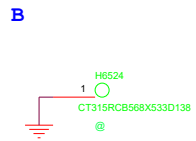
A: PCB Footprint :nbs_nut_1p_647
B: PCB Footprint :nbs_nut_1p_648

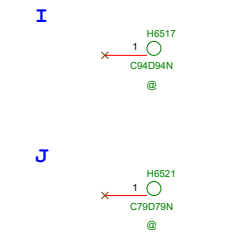


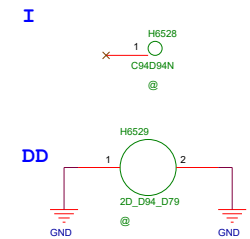


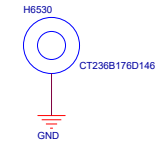


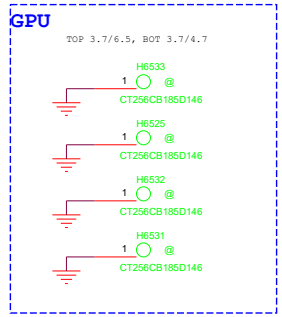


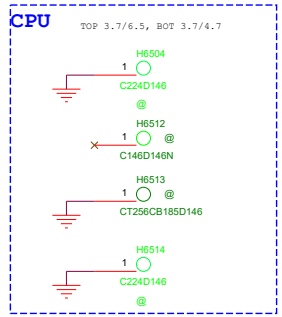












<Core Design>

ASUSTeK COMPUTER	Title : I/O board FUNC key	
	Engineer: EE	
Size: B	Project Name: GA503QS	Rev: 1.0
Date: Wednesday, March 17, 2021	Sheet 65 of 103	

Project Name

GX703_SD_SB

Rev

R1.0

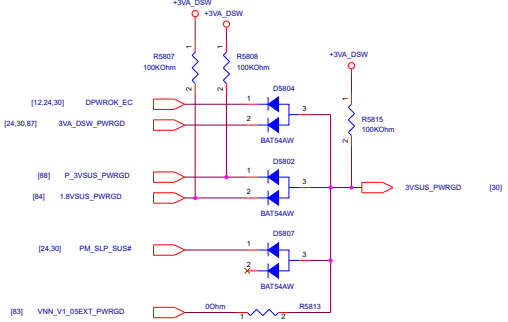
Title : CR_GL3232S

Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER INC.	TG_Wei

Date:	Sheet	of
Wednesday, March 17, 2021	66	103

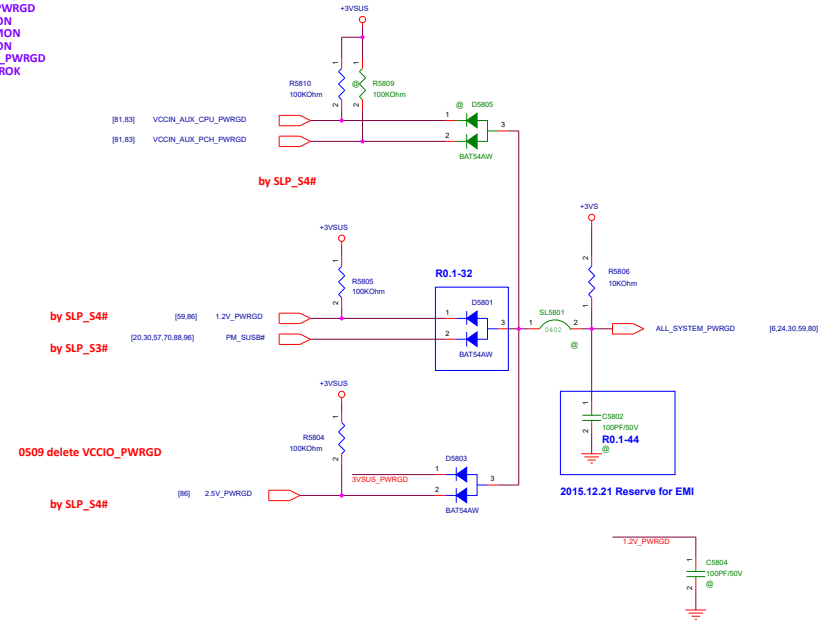
[SUS_VR_PWRGD]

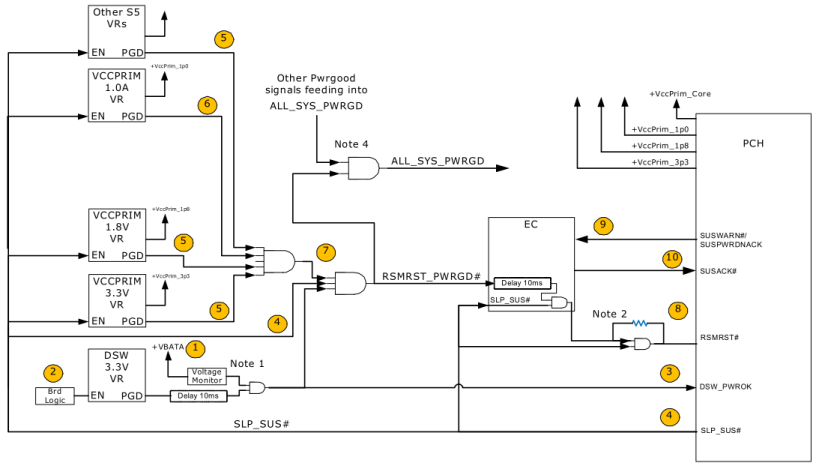
SLP_SUS_N
V0.85_PWRGD
V3.3A_V5A_PWRGD
V1.0A_PWRGD
V1.8A_PWRGD
DPWROK=3.3A_DSWPWRGD+10ms & BATT>5.35V

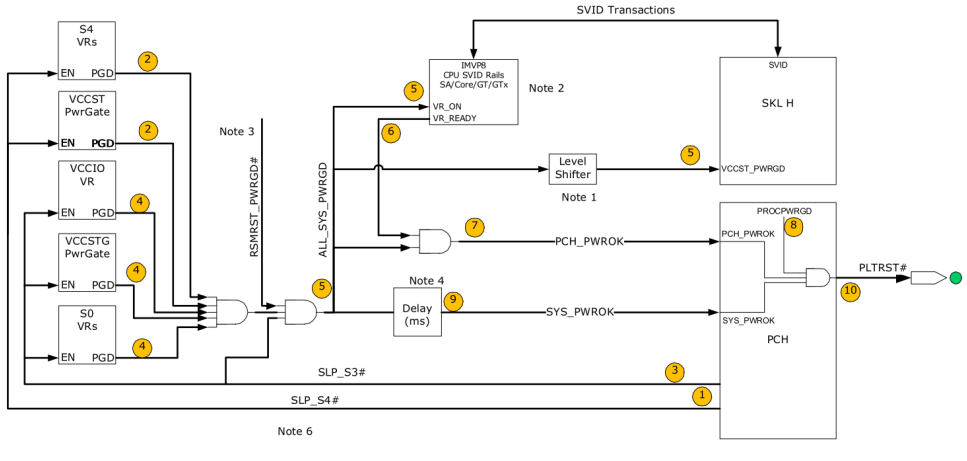


[ALL_SYSTEM_PWRGD]

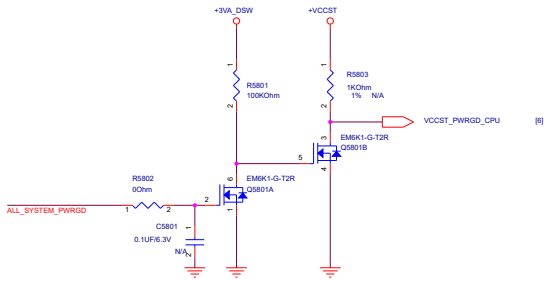
SLP_S3_N
DDR_PWRGD
VCCIO_PWRGD
3.3S_MON
1.00U_MON
1.8S_MON
RSMRST_PWRGD
SYS_PWROK



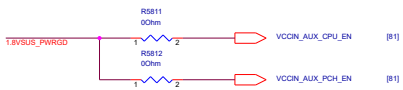




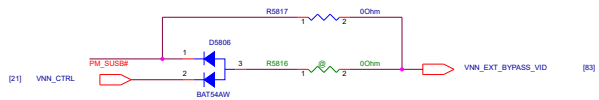
[VCCST_PWRGD for PCH]



[1.8VSUS_PWRGD for VCCIN_AUX enable]



[VID Control for VCC_VNNEXT_1P05/VCC_V1P05EXT_1P05]



VCC_VNNEXT_1P05 VR Voltage Configurations

VID1	
SLP_S3#	Output Voltage
0	1.05
1	0.78

VCC_1P05EXT : 1.05V(fixed)

VID2	Output Voltage
0	1.05
1	0.96

<Core Design>

ASUSTeK COMPUTER

Title : Power Protect

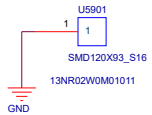
Engineer: EE

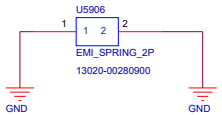
Size	Project Name	Rev
C	GX502GX	R1.2

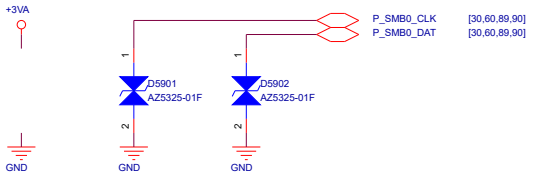
Date: Wednesday, March 17, 2021 Sheet 58 of 103

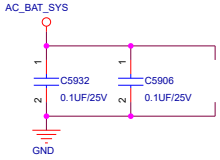
EMI SPRING (2.6H)*3 13NB0I50M01011

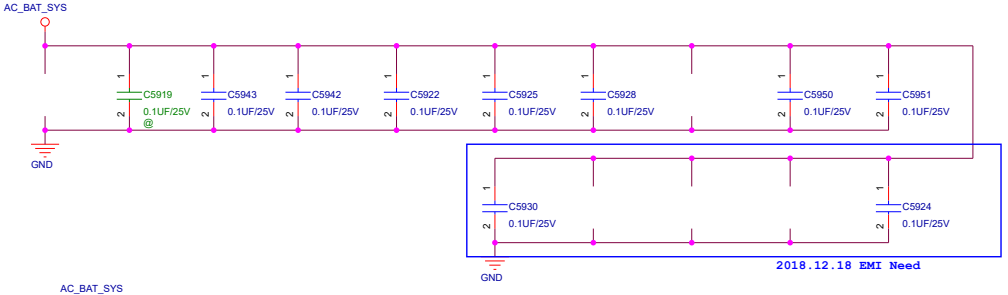
EMI SPRING (4.2H)*2 13NK00B1M01011
EMI SPRING (3.5H)*1 13GOK0F10M010-10

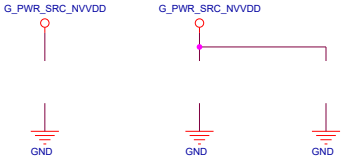


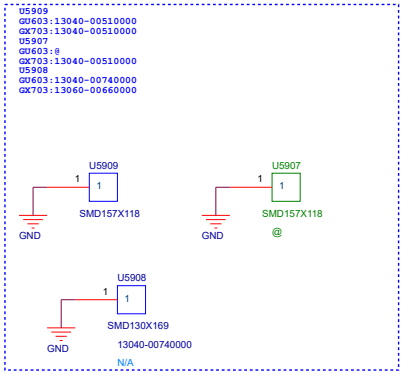


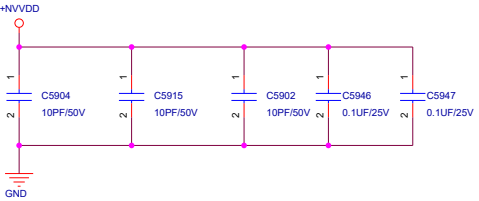


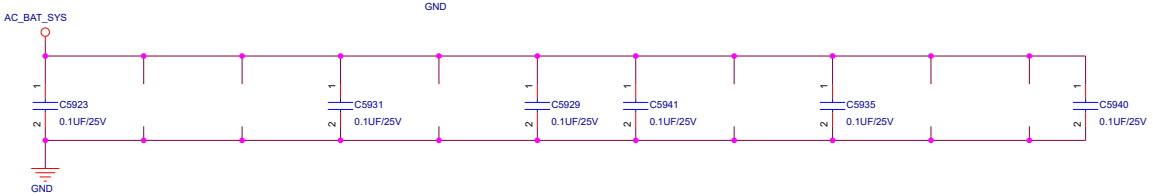


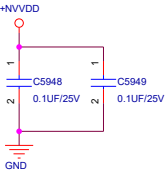


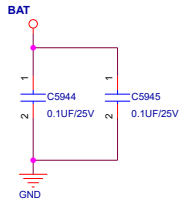


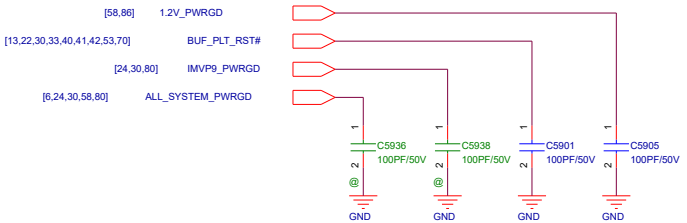


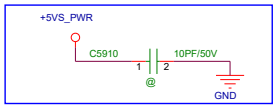






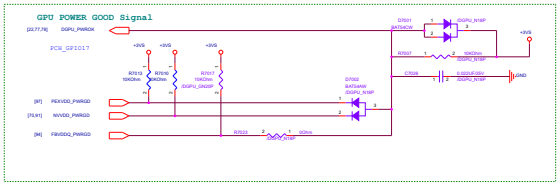






<Core Design>

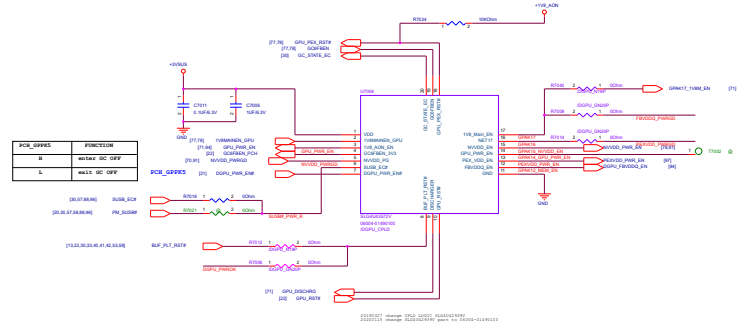
ASUSTeK COMPUTER	Title : I/O_Main board Conn.	
	Engineer: EE	
Size: B	Project Name: GX502GX	Rev: R1.2
Date: Wednesday, March 17, 2021	Sheet 59 of 103	

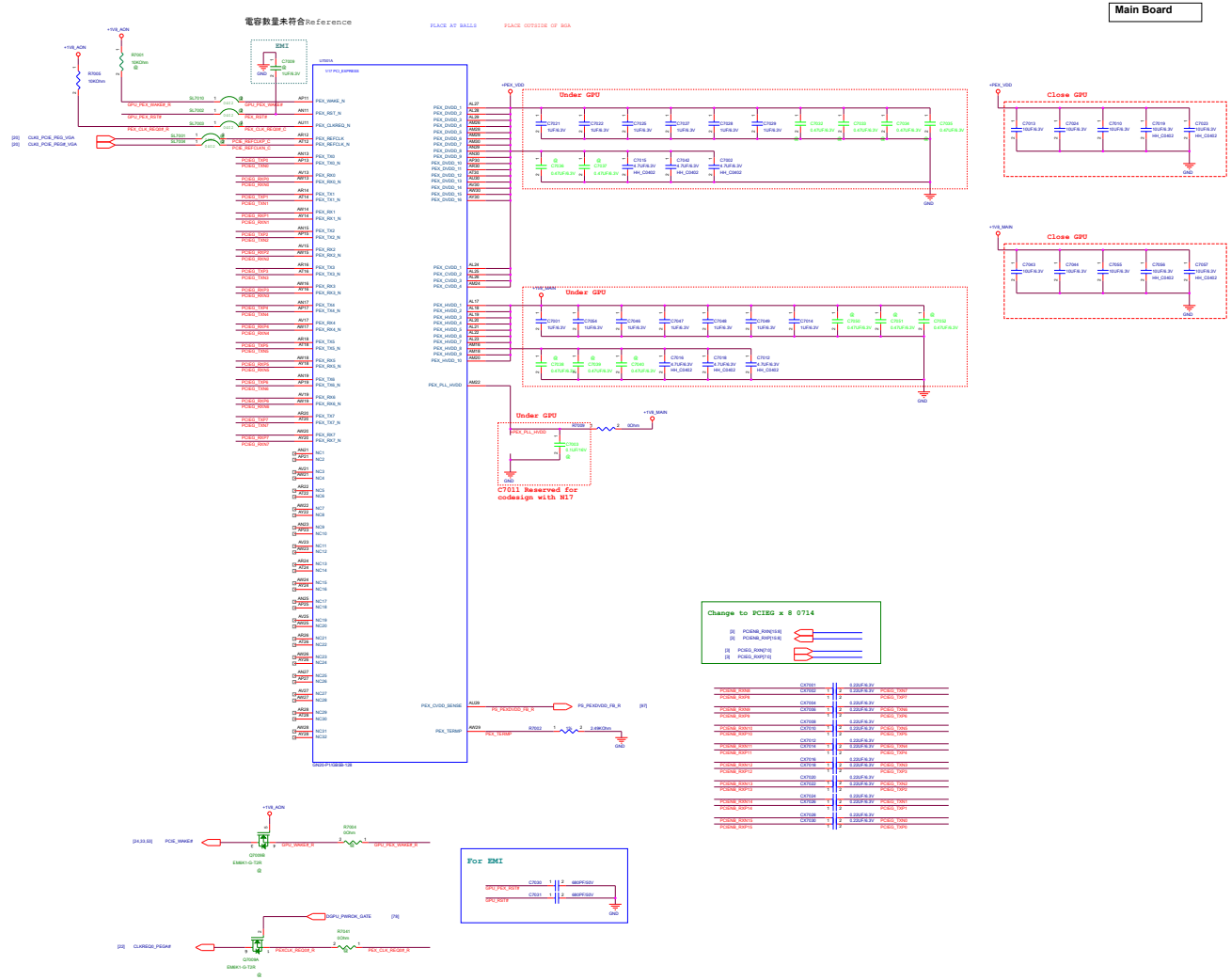


Optional	Part Reference	N18P Part number	GN20 Part number	Remark
/DGPU_GN20P	R7006, R7008, R7014, R7017, R7103, R7113, R7808, R7809, R7818			GN20P系列需要上件
/DGPU_N18P	D7002, D7001, R7007, R7012, C7026, R7040, R7023 U7102, C7159, C7161, C7113, R7101, R7149, R7124 R7841, R7821, R7864, R7813,R7831			GN18P-G61-A需要上件
/DGPU_CPLD	U7004	06004-01490100	06004-01650200	N18P與GN20P 使用CPLD對應料號
/DGPU_ROM	U7802	05006-00041600	05006-00072900	N18P與GN20P 使用ROM對應料號
/DGPU_VREF	R7205	10G21249R914010	10G212249114030	N18P與GN20P VREF的Pull down電阻不同
/VRAM				FOR GPU VRAM 的VG BOM

GPU POWER SEQUENCE CONTROL

PCH_GPIO65	FUNCTION
H	enter GC OFF
L	exit GC OFF





ASUS	Project Name: GX502GX		Rev: 30.2
Title : GPU PCIE1F			
Size: Custom	Dept.:	Engineer:	
Date: Wednesday, March 17, 2021	Sheet 79 of 103		

<Core Design>

Title : BT_Bluetooth

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A3	**GX502GX**	R1.2

Date:	Wednesday, March 17, 2021	Sheet	61	of	103

Title : NFC_CON_MB

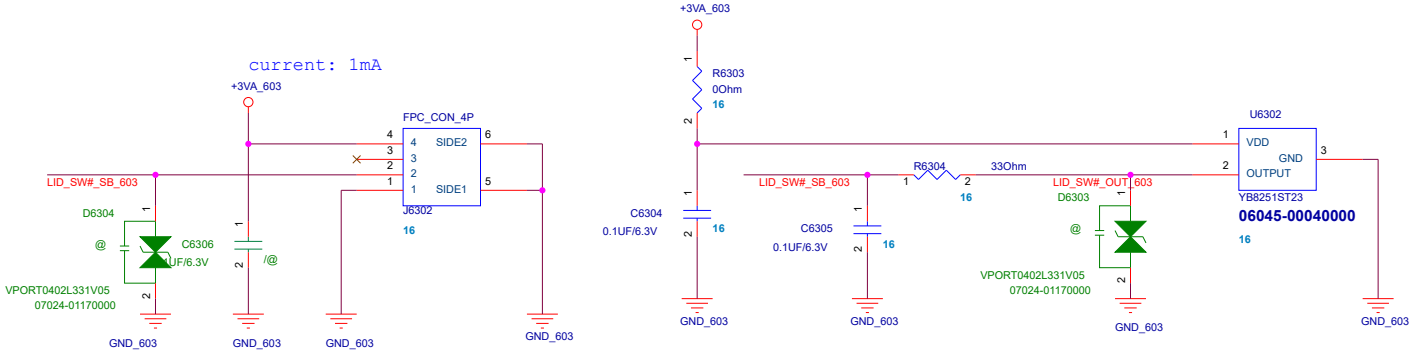
ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
B	**GX703_GU603**	R1.2

HALL SENSOR

GU603



<Core Design>

ASUSTeK COMPUTER INC. NB1	Title : Hall Sensor	
	Engineer: EE	
Size: Custom	Project Name: GX703_GU603	Rev: R1.0
Date: Wednesday, March 17, 2021	Sheet 63 of 103	

[72] FBB_D[31..0]

[72] FBB_CMD[24..0]

40 OHm_NET
FBB Partition 31..0

U74001

+FBVDDQ

MEM_VPP

121Ohm 2 1% 1 R74002 /GPU_KA

121Ohm 2 1% 1 R74001 /GPU_KA

GND GND

K4Z80325BC-HC14

/VRAM

[72] FBB_D[63..32]

[72] FBB_CMD[52..28]

40 OHm_NET
FBB Partition 64..32

U74002

+FBVDDQ

MEM_VPP

121Ohm 2 1% 1 R74004 /GPU_KA

121Ohm 2 1% 1 R74003 /GPU_KA

GND GND

K4Z80325BC-HC14

/VRAM

Integrated VREF reference

FBB_VREFC

R74005
1KOhm
/GPU_KB
1%

GND

<Variant Name>

Title	<Title>	
Size: C	Document Number: G512LI	Rev: R1.0
Date: Wednesday, March 17, 2021	Sheet 74 of 103	

<Variant Name>

Title <Title>		
Size A	Document Number G512LI	Rev R1.0
Date: Wednesday, March 17, 2021	Sheet 75 of 103	

Project Name

Type-A_USB3-10G

Rev

R1.0

Title : USB3.0 2 Port

Size	Dept.:	Engineer:
C	ASUSTeK COMPUTER INC.	

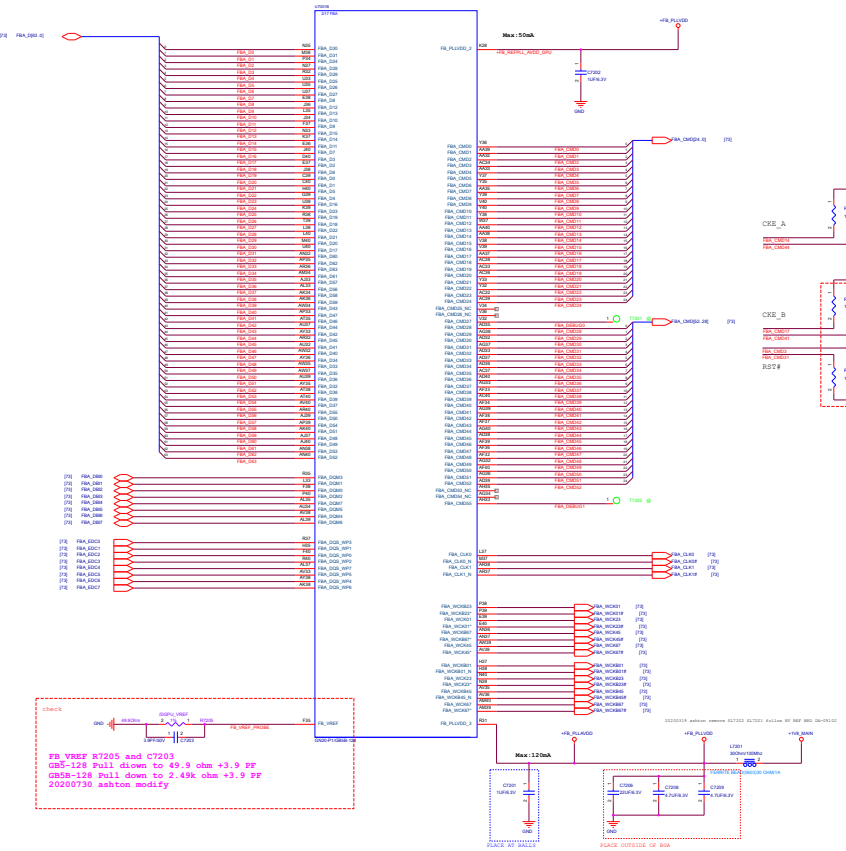
Date: Wednesday, March 17, 2021

ASUSTeK COMPUTER	Title : OTH_for test only	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: R1.2
Date: Wednesday, March 17, 2021	Sheet 68 of 103	

<Variant Name>

Title <Title>		
Size C	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, March 17, 2021	Sheet 69 of 103	

MEMORY: GPU FB Partition A



MEMORY: GPU FB Partition B

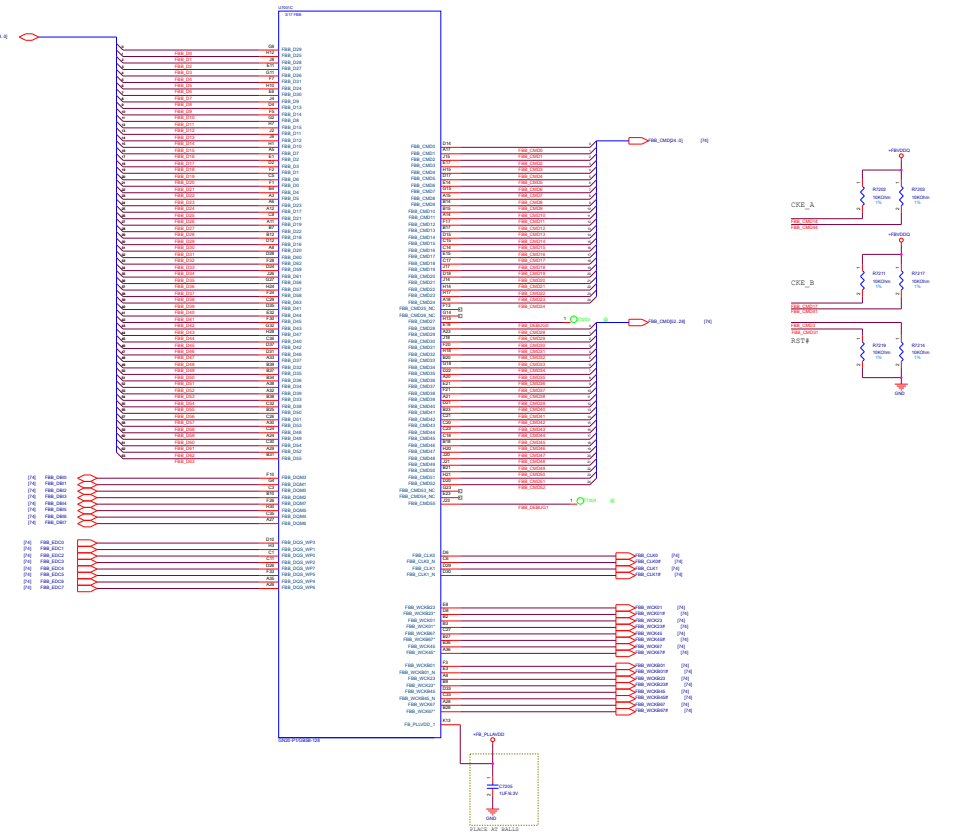


Table 13. GB5-128 and GB5B-128 FB BOM Differences

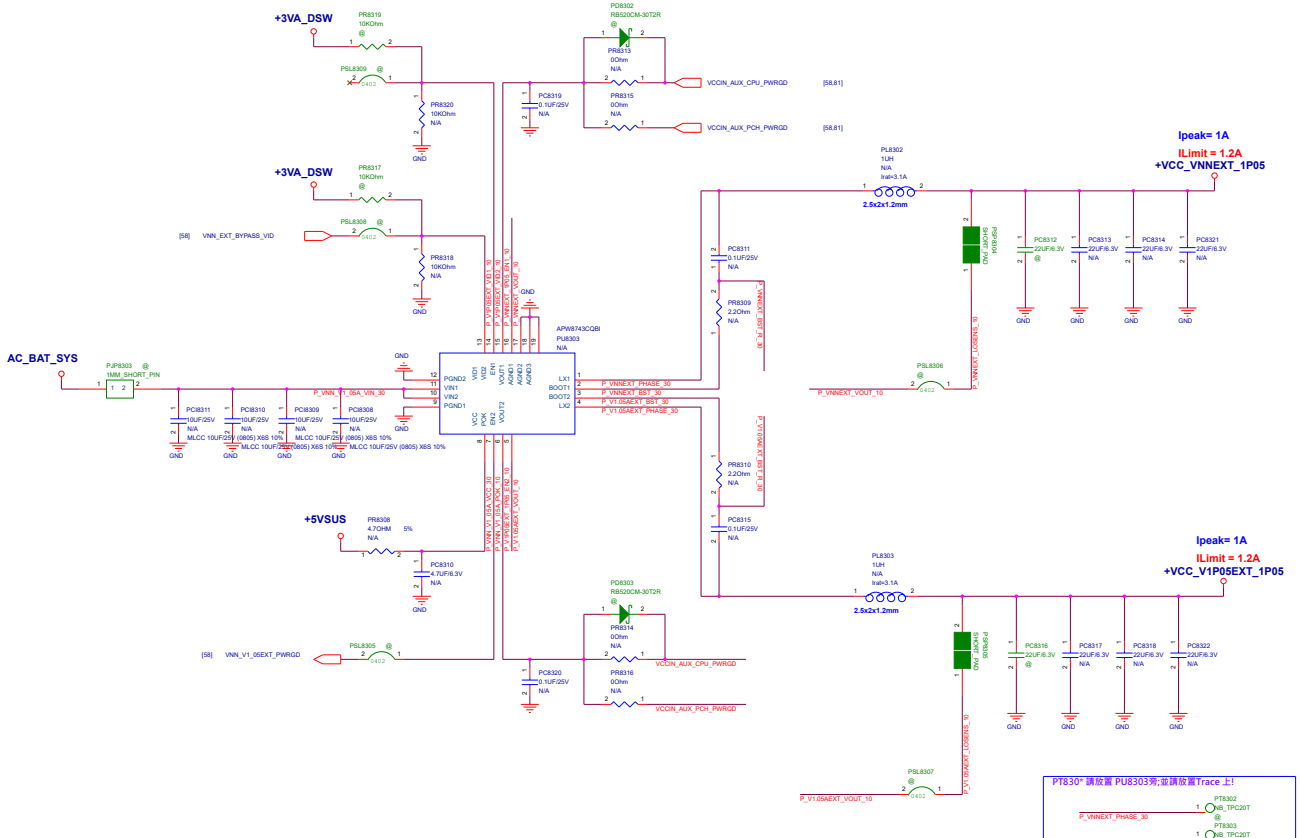
FB Pin	What to do for GB5-128	What to do for GB5B-128
FB_VREF	Pull down to 49.9 ohm + 3.9 pF Refer to *N18P-G61-A GeForce GPU Platform Development Package* (PDP-09900-001)	Pull down to 2.49 kΩ + 3.9 pF

Chih-Yu Chiu
ASUSTeK COMPUTER INC.

ASUS	Project Name: G512LI		Rev: R1.0
Title: GPU_FRAME BUFFER			
Size: D	Dept.: ASUSTeK COMPUTER	Engineer: NR EE RD3	
Date: Wednesday, March 17, 2021	Sheet: 72 of 163		

+1.05VSUS [For PCH]

+VCC_VNNEXT_1P05 / +VCC_V1P05EXT_1P05 [For PCH]

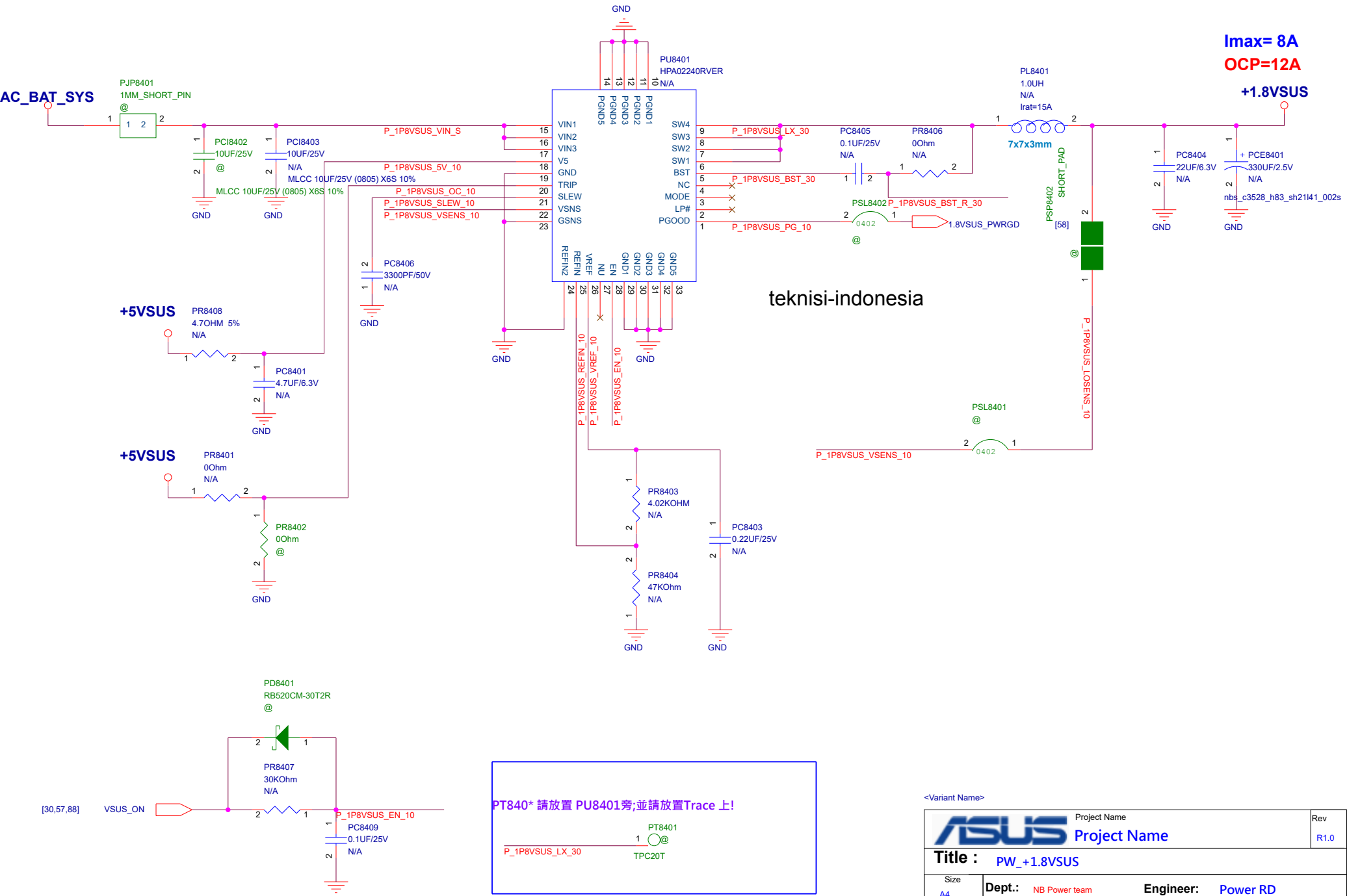


ASUS	Project Name: Tiger Lake-H		Rev: R1.0
Title :	PW_+1.05VSUS		
Size: A2	Dept.: NB Power team	Engineer: Power RD	
Date: Wednesday, March 17, 2021	Sheet 83 of 103		

<Variant Name>

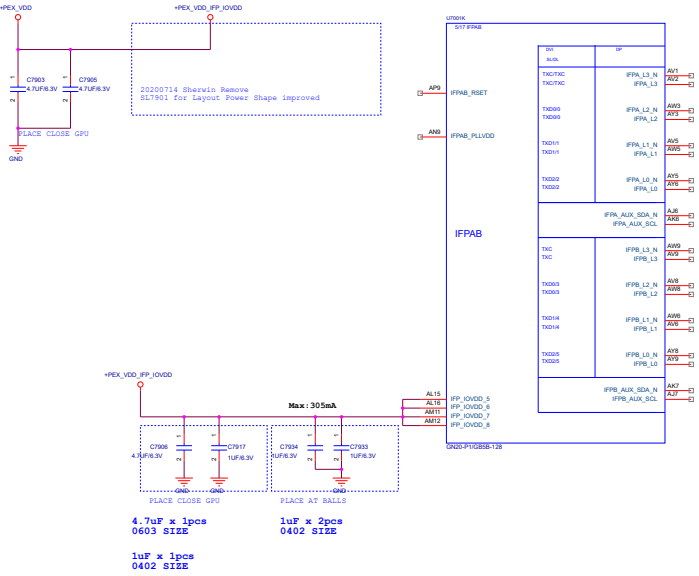
Title <Title>		
Size A	Document Number G512LI	Rev R1.0
Date: Wednesday, March 17, 2021	Sheet 76 of 103	

+1.8VSUS [For PCH]

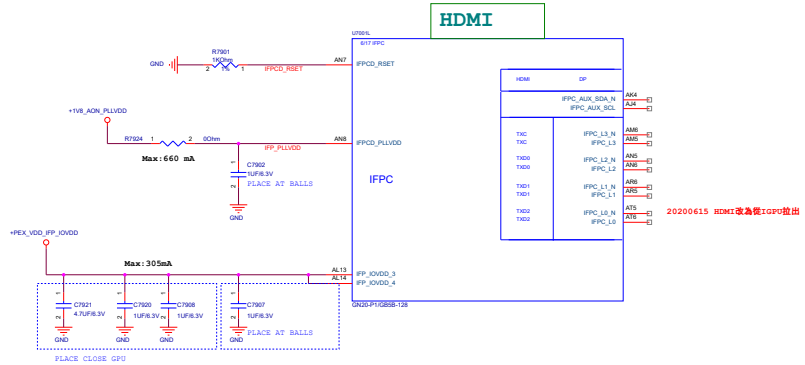


<Variant Name>

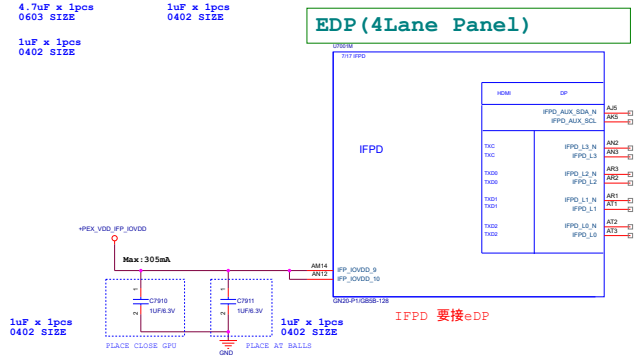
Project Name: Project Name		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Wednesday, March 17, 2021	Sheet 84 of 103	



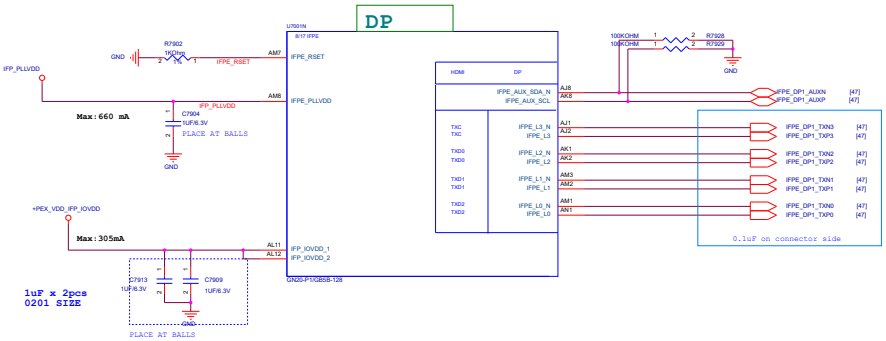
HDMI



EDP(4Lane Panel)



DP



ASUS	Project Name: GX502GX		Rev: R1.2
Title : GPU_DP/EDP/HDMI/LVDS/CRT			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet 79 of 103		

<Core Design>

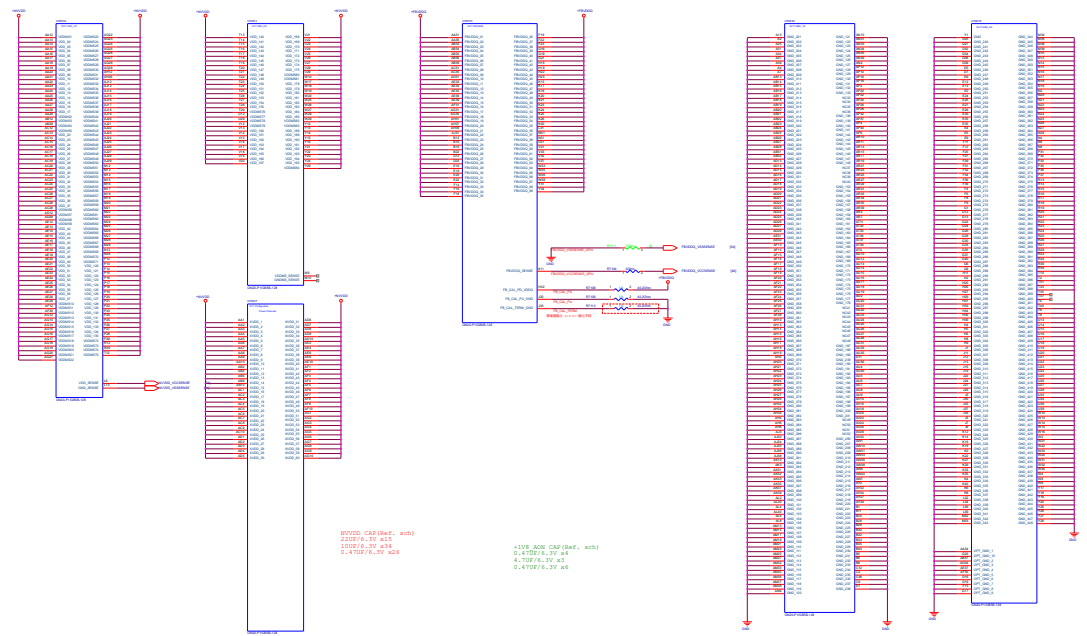
Title : OTH_for test only

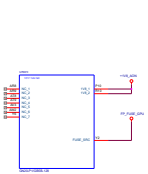
ASUSTeK COMPUTER

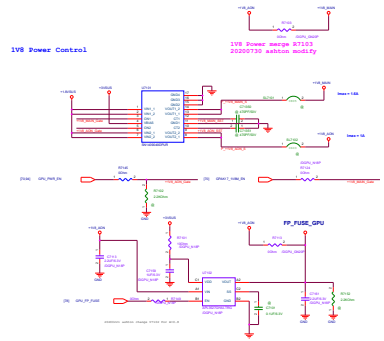
Engineer: EE

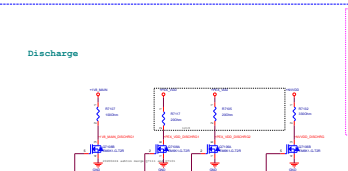
Size	Project Name	Rev
A	GX502GX	R1.2

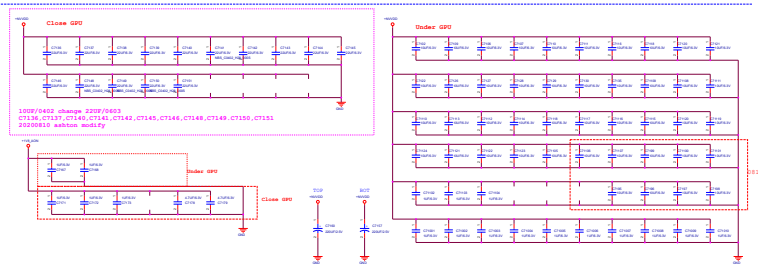
Date:	Wednesday, March 17, 2021	Sheet	85	of	103











ASUS	Project Name: G512LI		Rev: 1.0
Title: GPU POWER			
Size:	Document Number:	Engineer: Ashton_yang	
Date: Tuesday, May 07, 2019	Sheet:	of	

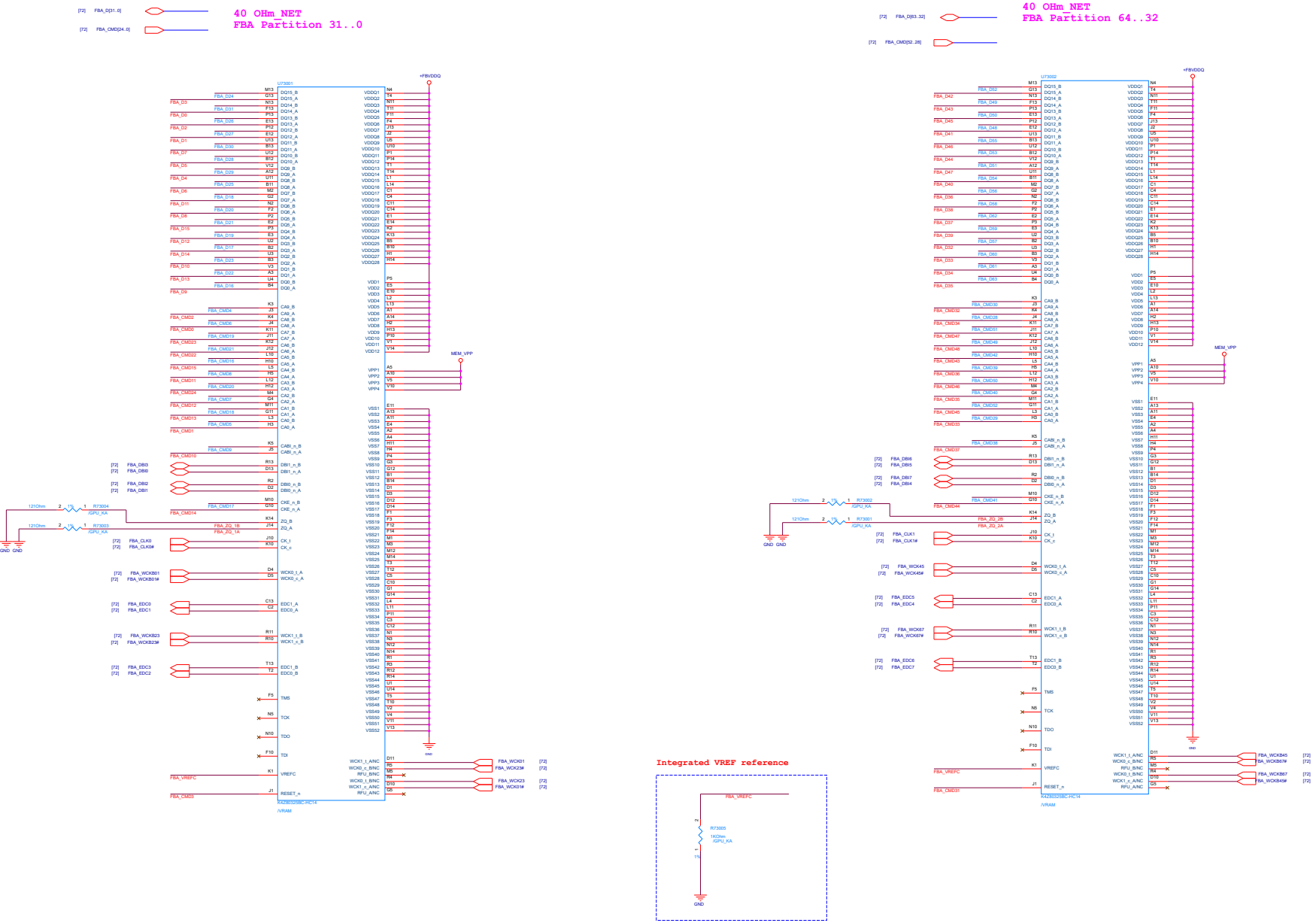


Table 4. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	Yes, TBD[2]	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	Yes, TBD[2]	Full	Production candidate

Notes:
1. For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
2. Requires Production GDDR6 with a specific date code restriction. Exact date code is currently TBD.

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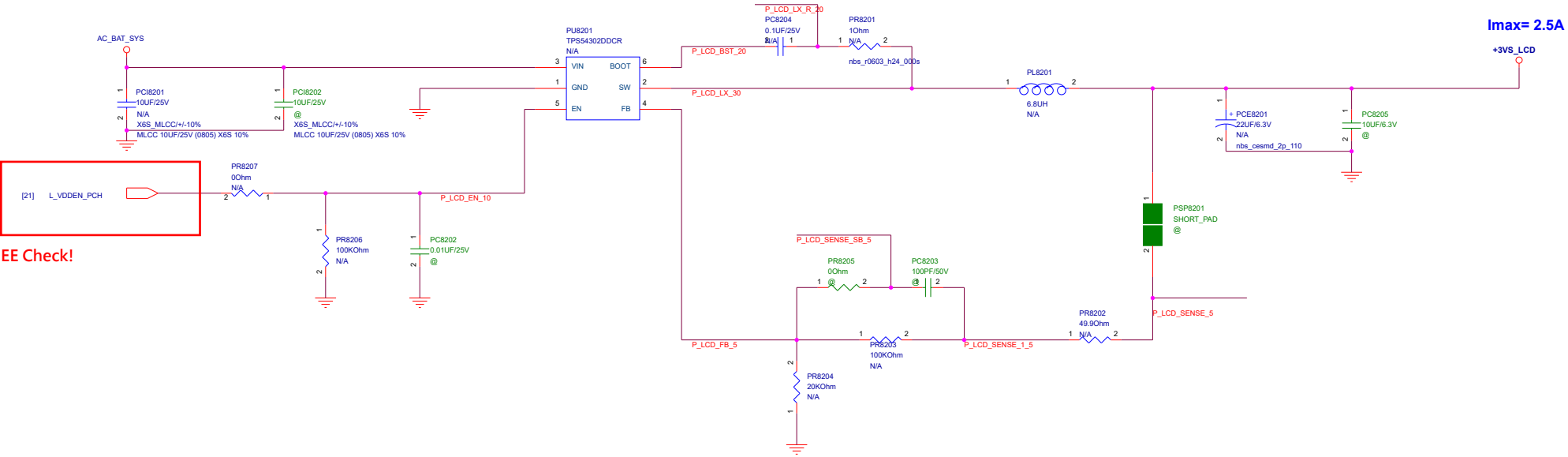
+3VS_LCD



<Variant Name>

ASUS	Project Name: Project Name	Rev: R1.0
Title : PW_+3VS_LCD		
Size: A3	Dept.: NB Power team	Engineer: Power RD
Date: Wednesday, March 17, 2021	Sheet 82 of 103	

Load Switch

Main Board

uP9030 ILIM/LPM Setting 對應表		
ILIM PIN	LPM (C10)	LIMIT Current
GND	Off	3A
1M to GND	Off	5A
Float/VDD	On	8A

PR8838 & PC8838 close VDD PIN

Imax = 0.0201A
+3VA_EC

Imax = 3.45A
+3VSUS

Check pull high with EE

Imax = 2.821A
+5VS
+5VS_PWR
PSL8808請放置PQ8804旁

LSW並聯使用, 注意擺件與VIN&Vo Shape

Imax = 7.92A
+3VS
+3VS_PWR
PSL8809請放置PU8807、PU8809與Vo MLCC
PC8833或PC8842旁

Check EN with EE

Imax = 0.97A
+VCCSTO
+VCCST

Imax = 0.34A
+VCCSTG

Imax = 0.5A
+VCC1P8A

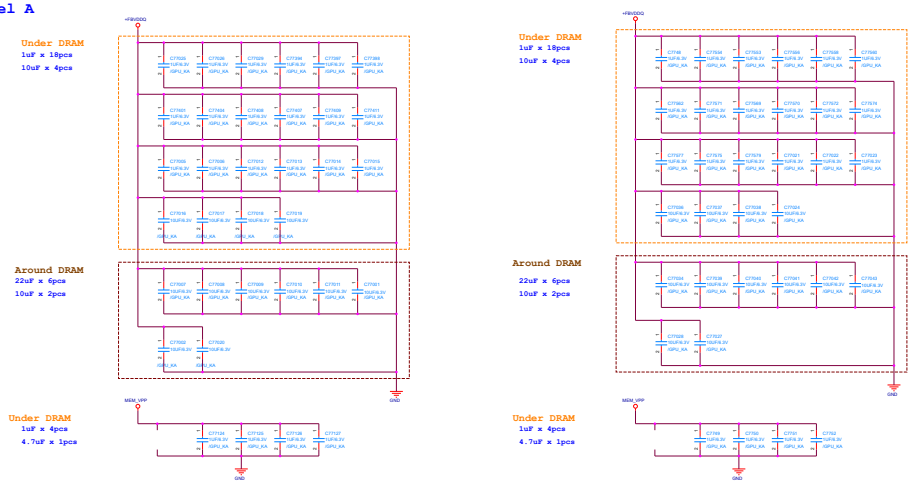
+VCC1P8AO

+12VS 的 Vin 對應 BOM 表		
	+12VS_FAN	+12VSUS
PR8821	N/A	@
PR8826	@	N/A
PQ8814	@	N/A

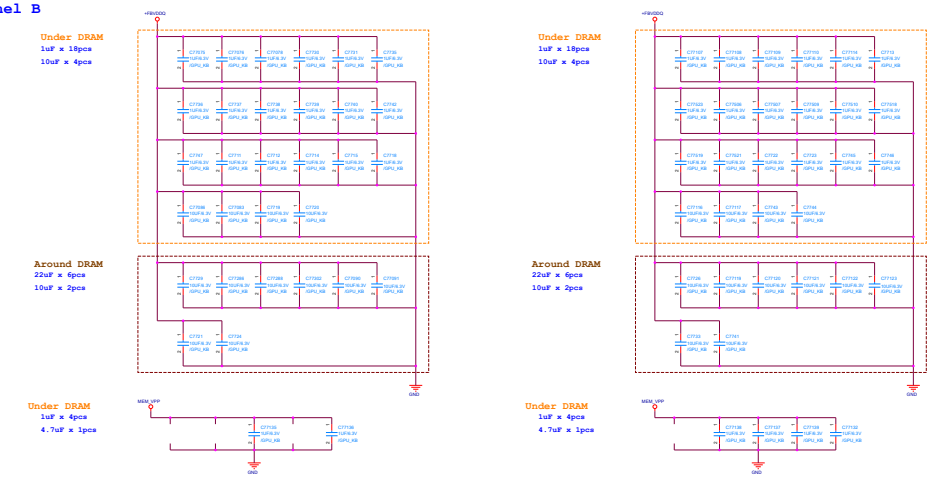
Project Name	Tigerlake-H	Rev	R1.0
Title :	PW_LOAD SWITCH		
Size	A2	Dept.:	NB Power team
Engineer:	Neil		
Date:	Wednesday, March 17, 2021	Sheet	88 of 103

FBVDDQ/VPP (VRAM)

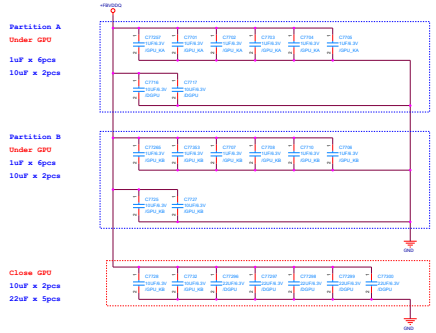
Channel A



Channel B



FBVDDQ (GPU)



FBVDDQ (GPU side)[1]	1.35V 1.5V	24 x 0.47uF (0201W X6S) 4 x 10uF (0603 X6S) - - - - - - - - - - - - - - - - - Alternate solution: 12 x 1uF (0402 or 0201W, X6S)[3] 4 x 10uF (0603 X6S)	2 x 10uF (0603 X6S)[2] 5 x 22uF (0603 X6S)

Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size NOTE 1]	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF NOTE 2	X6S [0201W]	36	Under or very close to DRAM
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Around DRAM
22 uF	X6S [0603]	6	
VPP Rail			
0.47 uF NOTE 3	X6S [0201W]	4	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

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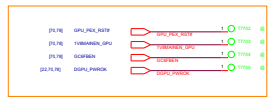
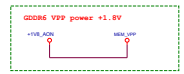
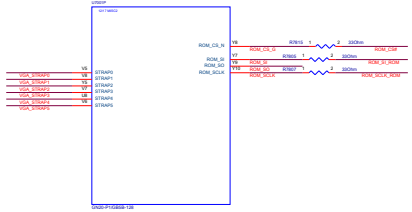
teknisi-indonesia

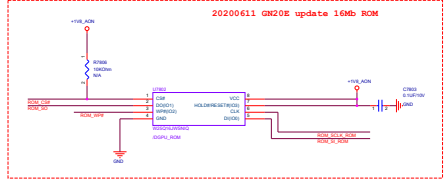
For power sequence measurement

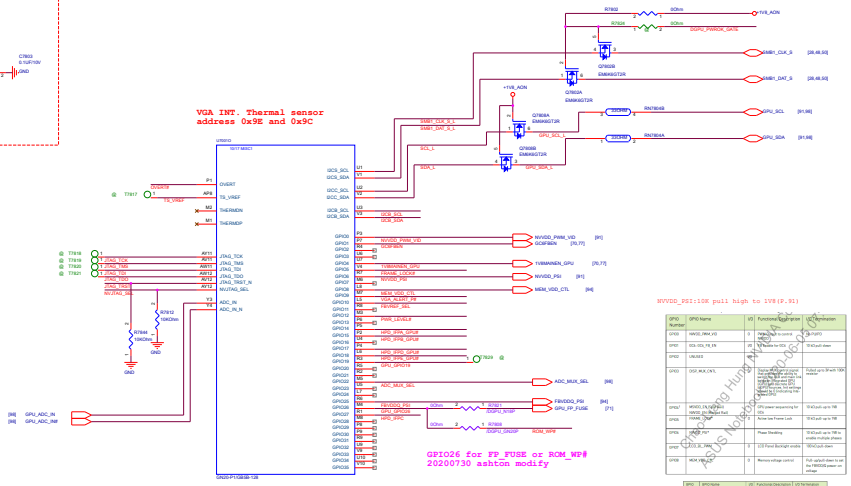


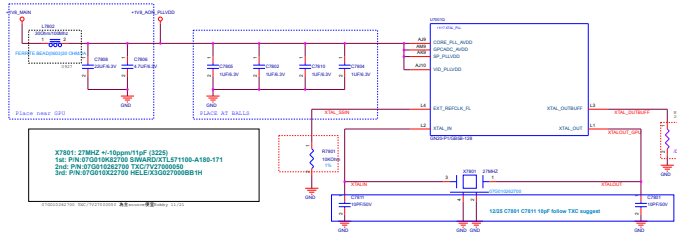


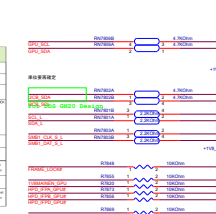
20200319 ashton remove SLC701 follow HV REF BRD SA-09122

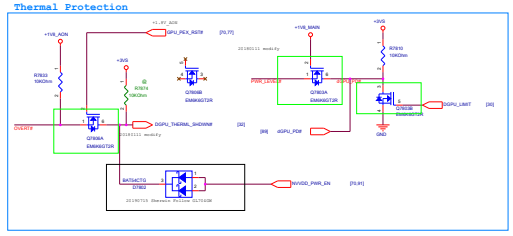


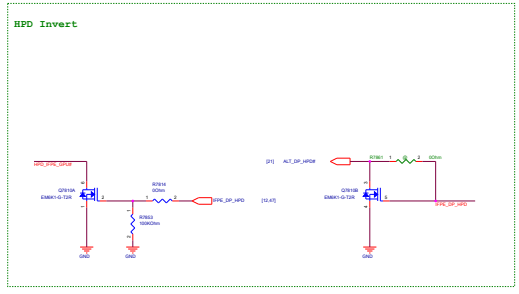


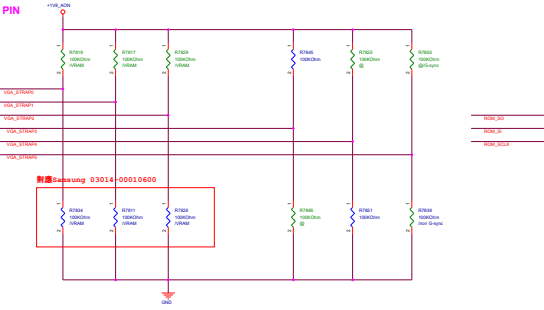












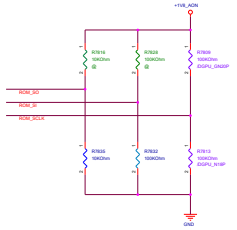


Table 9.1 Ternary Strap Levels

Level Option	Physical Configuration	
	Pull-Up to 1.8V via resistor Note 1	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 100K Ohms. 1.8V rail and GND rail levels are able to within 5% are acceptable.

The FS_OVERT* strap should be configured to ENABLE the Failsafe_OVERT* function. See the L-L-H row of Table 9.6.

Table 9.6 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
see Note 2			
L	L	L	FS_OVERT* function DISABLED
H	H	H	FS_OVERT* function ENABLED
all other configurations			Unstable, do not configure

DEFULT : L L H

ASUS P/N	Memory Density	Vendor	Manufacturer Part Number	Strap	STRAP 0	STRAP 1	STRAP 2
GDDR6							
03014-00010600	8Gb	Samsung	K4Z80325BC-HC14	0X0	L	L	L
03014-00010900	8Gb	Hynix	H56C8H24AIR-S2C	0X2	L	H	L

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	M	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
M	L	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	1	0
L	L	M	0	0	M	0
L	H	L	0	1	0	0
L	H	H	0	1	1	0
L	H	M	0	1	M	0
L	M	L	1	0	0	0
L	M	H	1	0	1	0
L	M	M	1	0	M	0
M	L	L	1	1	0	0
M	L	H	1	1	1	0
M	L	M	1	1	M	0
M	H	L	1	0	0	1
M	H	H	1	0	1	1
M	H	M	1	0	M	1
M	M	L	1	1	0	1
M	M	H	1	1	1	1
M	M	M	1	1	M	1

Assorted Configuration Straps:-
1. SMB_ALT_ADDR Enable:- "0"-Signal GPU setting I2C address 0x9E, "1"-Dual GPU setting I2C address 0x9E, used when a second GPU
2. DEVID_SEL: G-sync function -> "0" normal GPU ID, "1" support G-sync GPU ID-
3. PCIE_CFG: PCIE Swing -> "0" PCIE Swing default, "1" PCIE swing reduce-
4. VGA_DEVICE: Graphics circuit -> "0" MS-Hybrid, "1" Discrete-

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

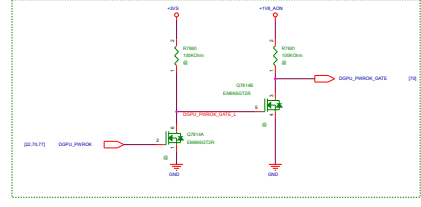
DEFULT : L L H

GPU GPIO INPUT

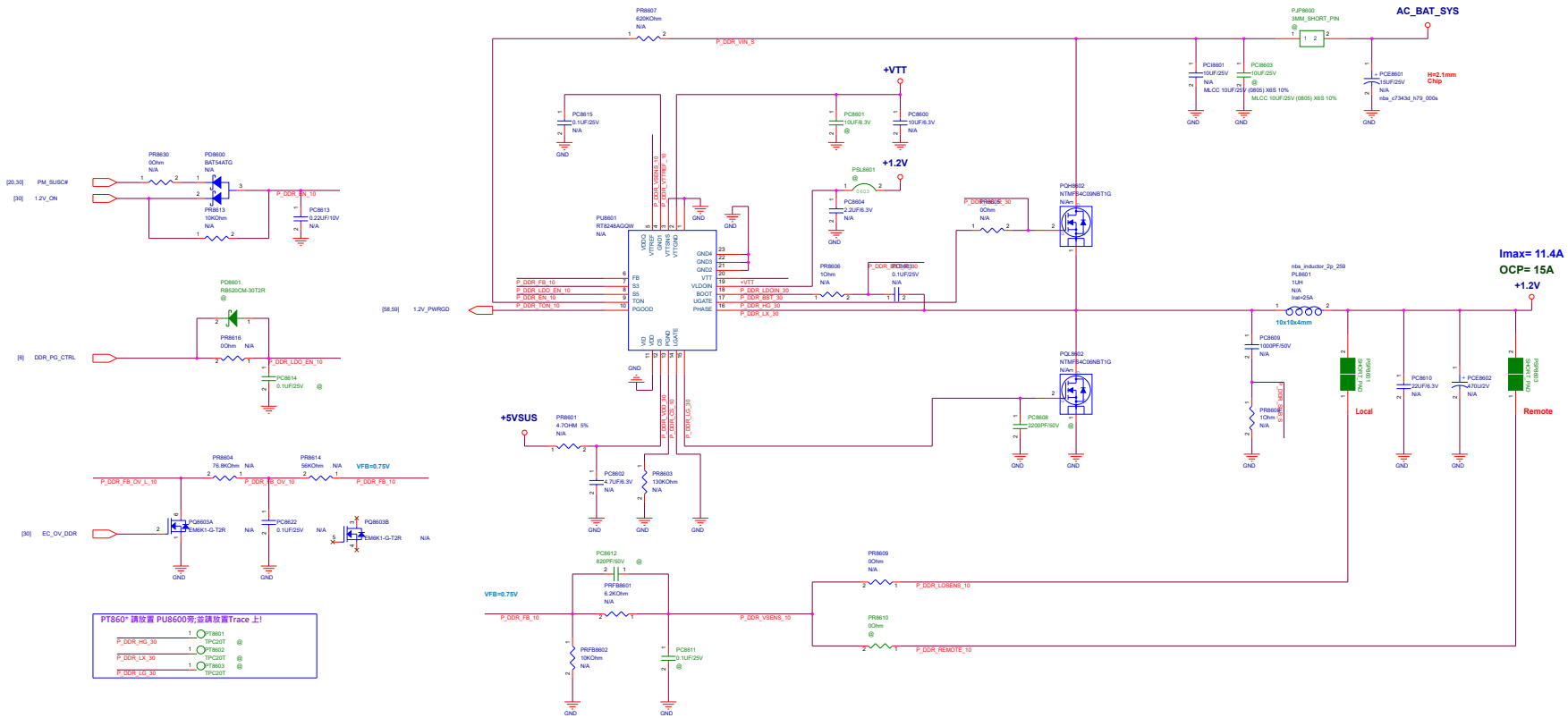
NVIDIA GC6 2.0 follow DG-07720-001_v01
GPU_GPIO 5 --> FRAME_LOCK# (Input, Open Drain)
High-->driver display ,Low Normal

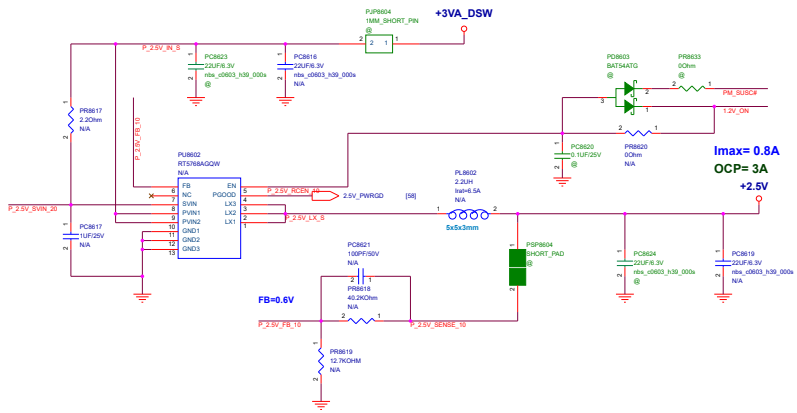
FRAME_LOCK#_C Pull High +3VS_LCD at Panel side

For EMI



+1.2V / +VTT / +2.5V[For Memory]



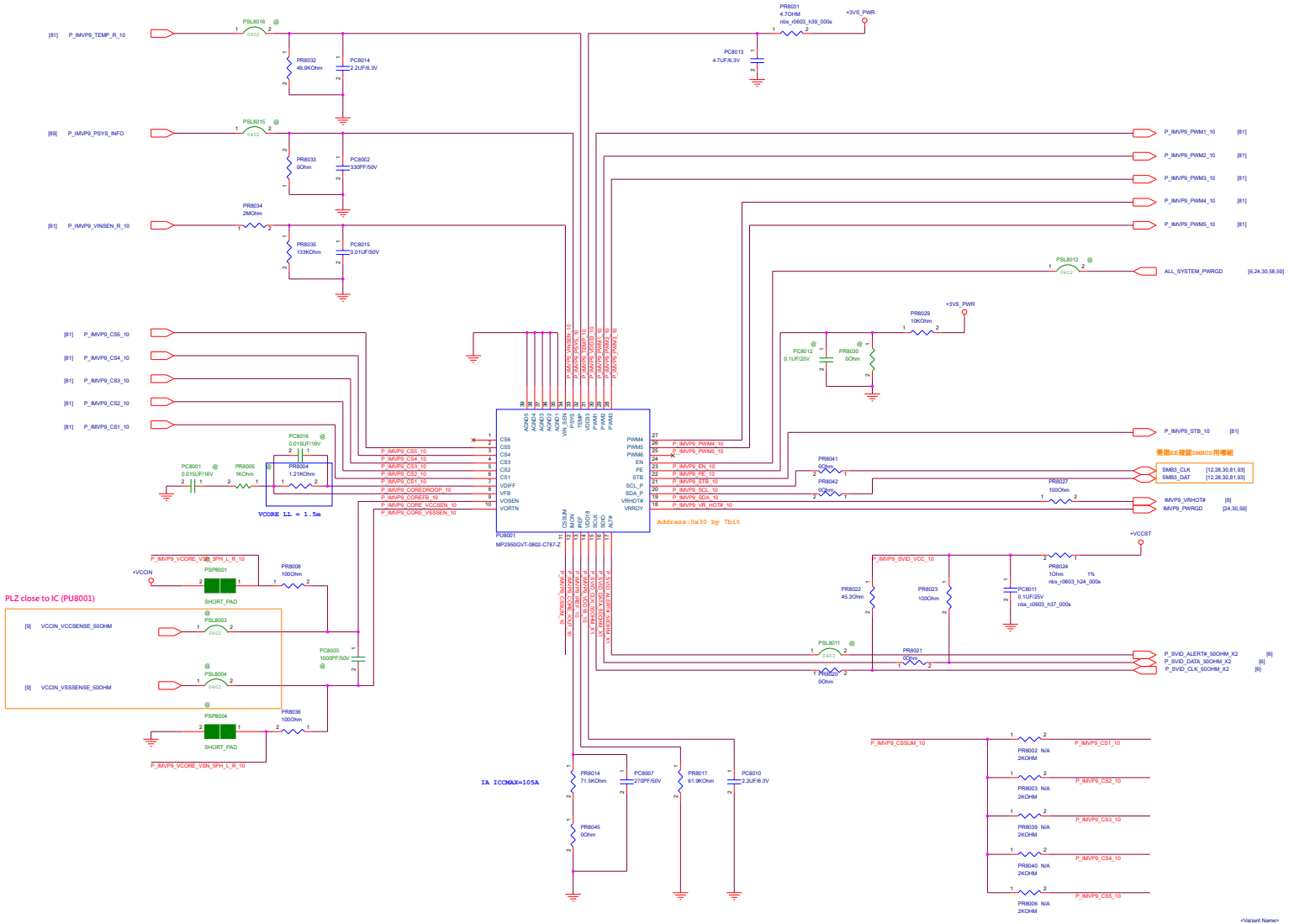


<Core Design>

ASUS	Project Name: Tiger Lake-H		Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: NB Power team	Engineer: Power RD	
Date: Wednesday, March 17, 2021	Sheet 86 of 103		

Tiger Lake-H IMVP9 Power (1) [For CPU]

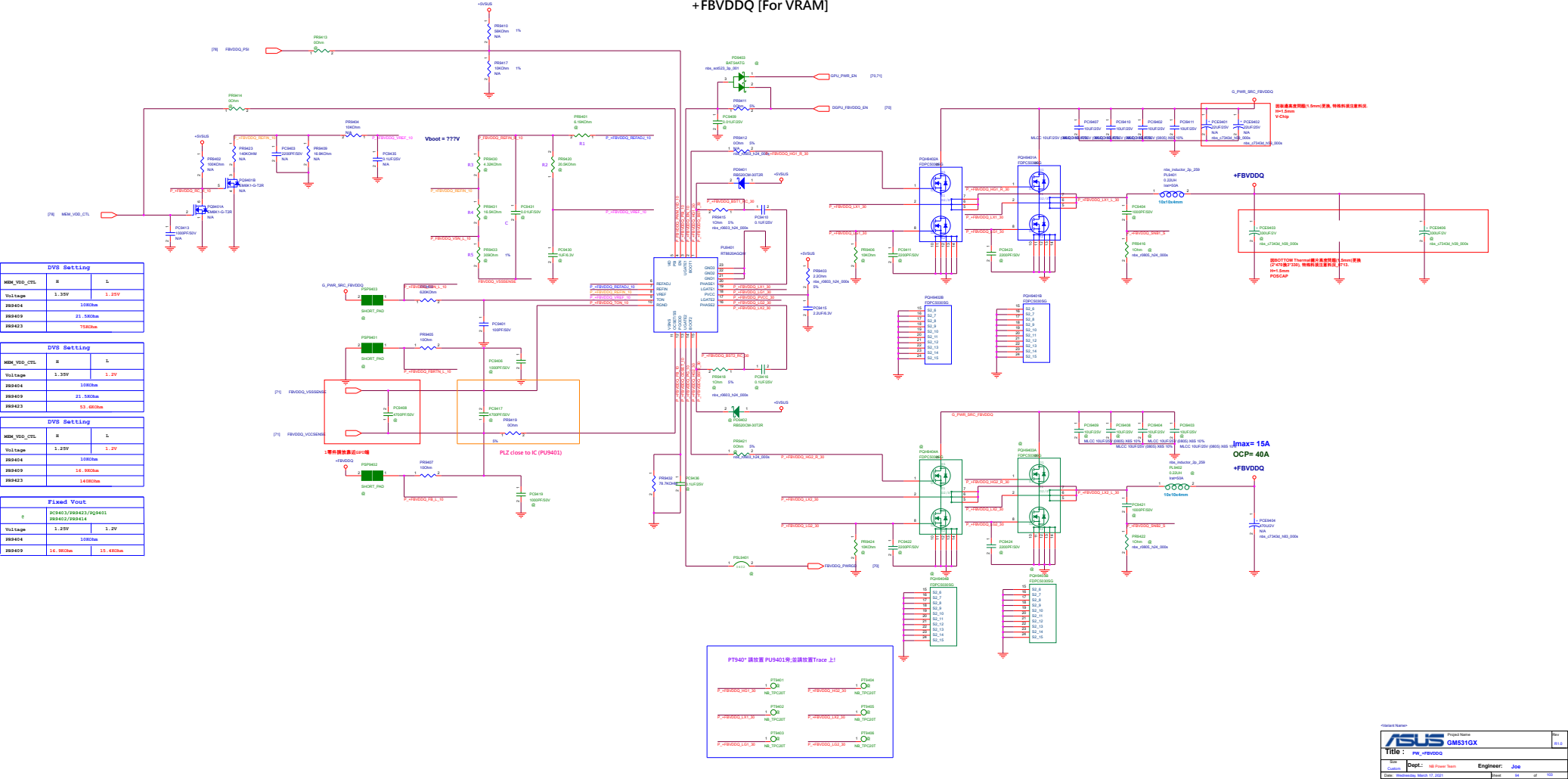
PR8033	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm



<Variant Name>

ASUS	Project Name: G533	Rev: R1.0
Title : PW_TIGERLAKE (1)		
Size: Custom	Dept.: NB1-RD3EE1	Engineer: Joe
Date: Wednesday, March 17, 2021	Sheet: 80 of 103	

+FBVDDQ [For VRAM]



DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
9R9404	10KOhm	
9R9409	21.5KOhm	
9R9423	75KOhm	

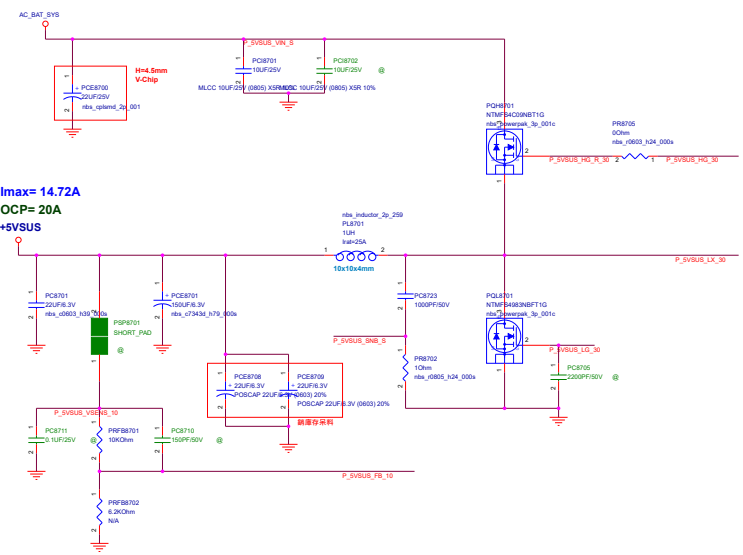
DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.2V
9R9404	10KOhm	
9R9409	21.5KOhm	
9R9423	53.6KOhm	

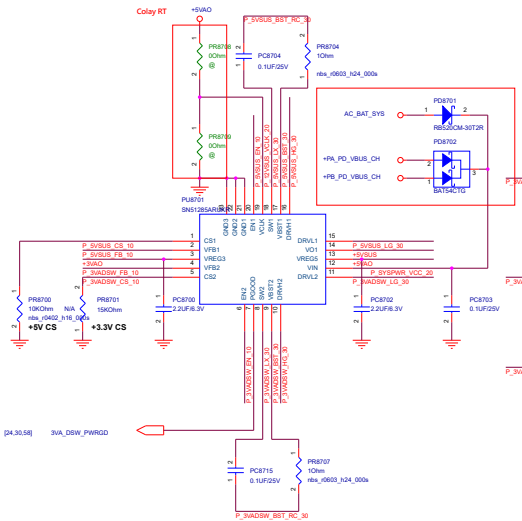
DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.25V	1.2V
9R9404	10KOhm	
9R9409	16.9KOhm	
9R9423	140KOhm	

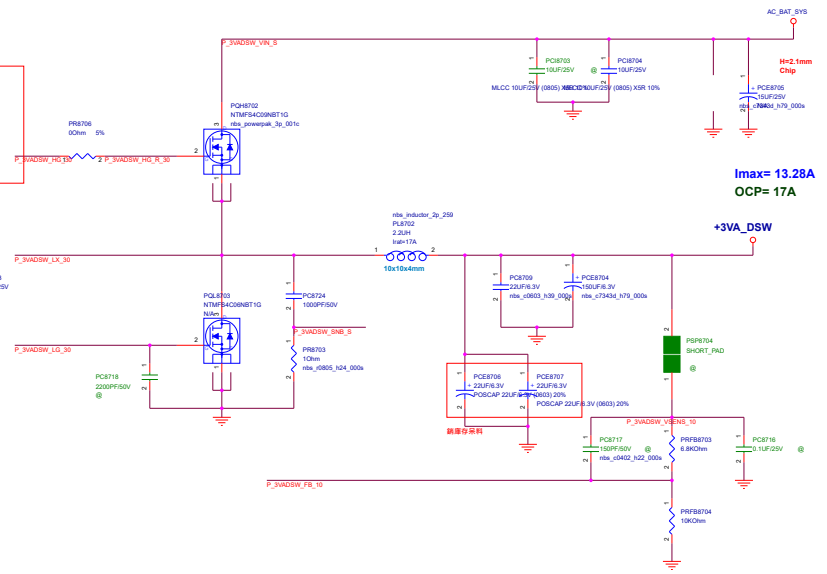
Fixed Vout		
@	PC9403/9R9423/BQ9401 9R9402/9R9414	
Voltage	1.25V	1.2V
9R9404	10KOhm	
9R9409	16.9KOhm	15.4KOhm

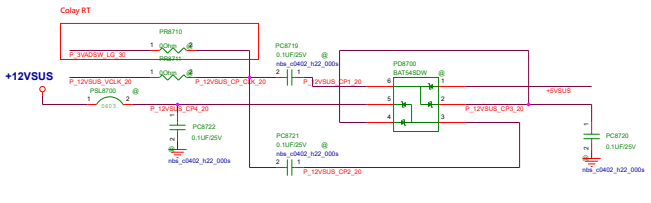
<Variant Name>		
ASUS	Project Name: GM531GX	Rev: R1.0
Title :	PW_+FBVDDQ	
Size: Custom	Dept.: NB Power Team	Engineer: Joe
Date: Wednesday, March 17, 2021	Sheet: 94 of 103	

+3VA_DSW / +5VSUS [System Power]

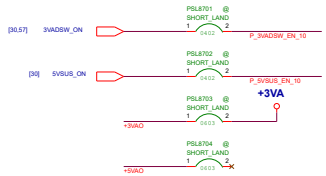








請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



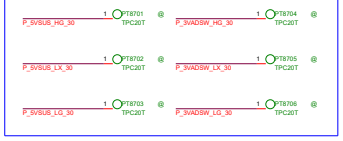
Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

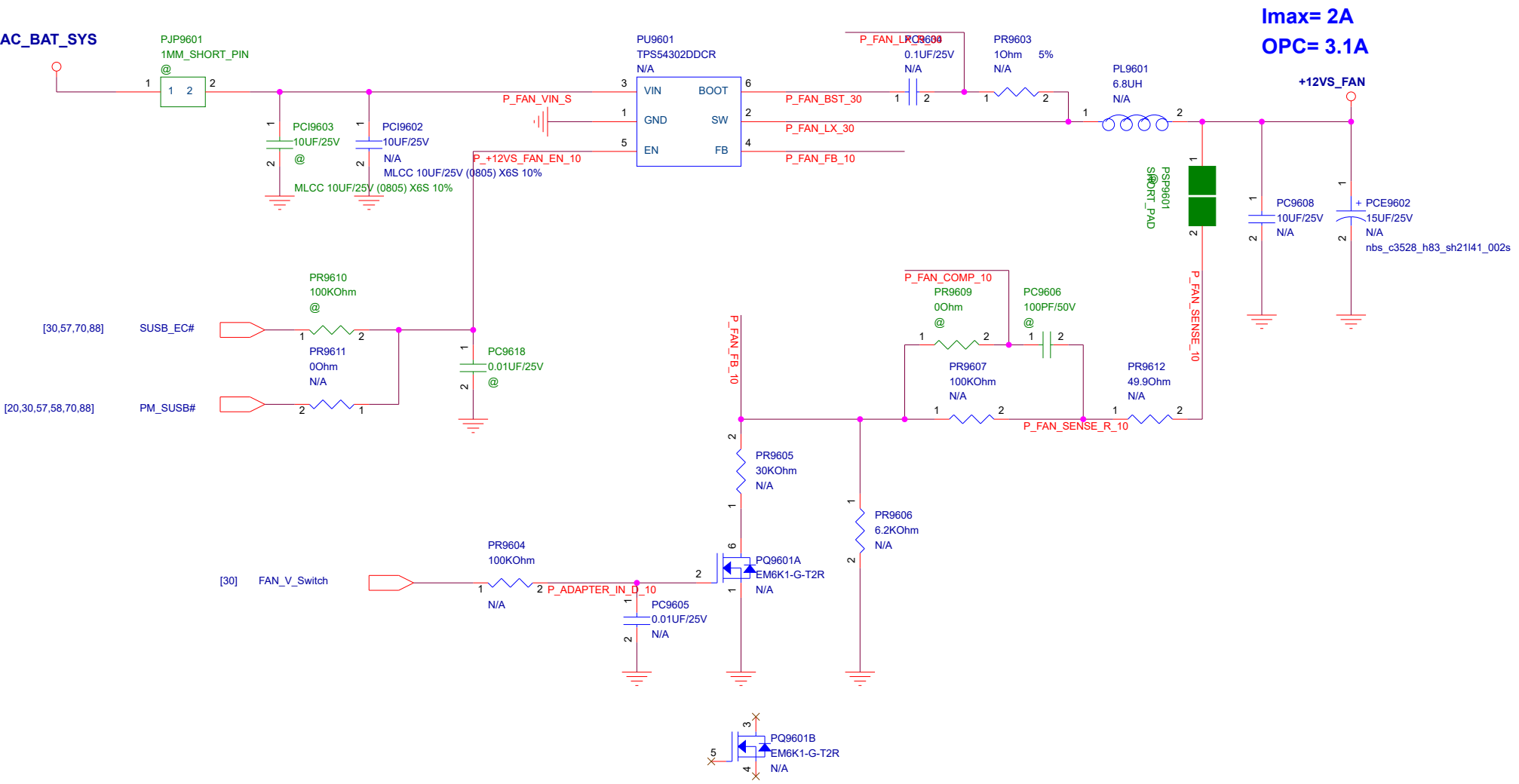
PT870* 請放置 PU8700旁;並請放置Trace 上!



<Core Design>

ASUS	Project Name: GX502GX	Rev: R1.2
Title : PW_+3VA_DSW/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Joe
Date: Wednesday, March 17, 2021	Sheet 87 of 103	

+12VS_FAN [For FAN]

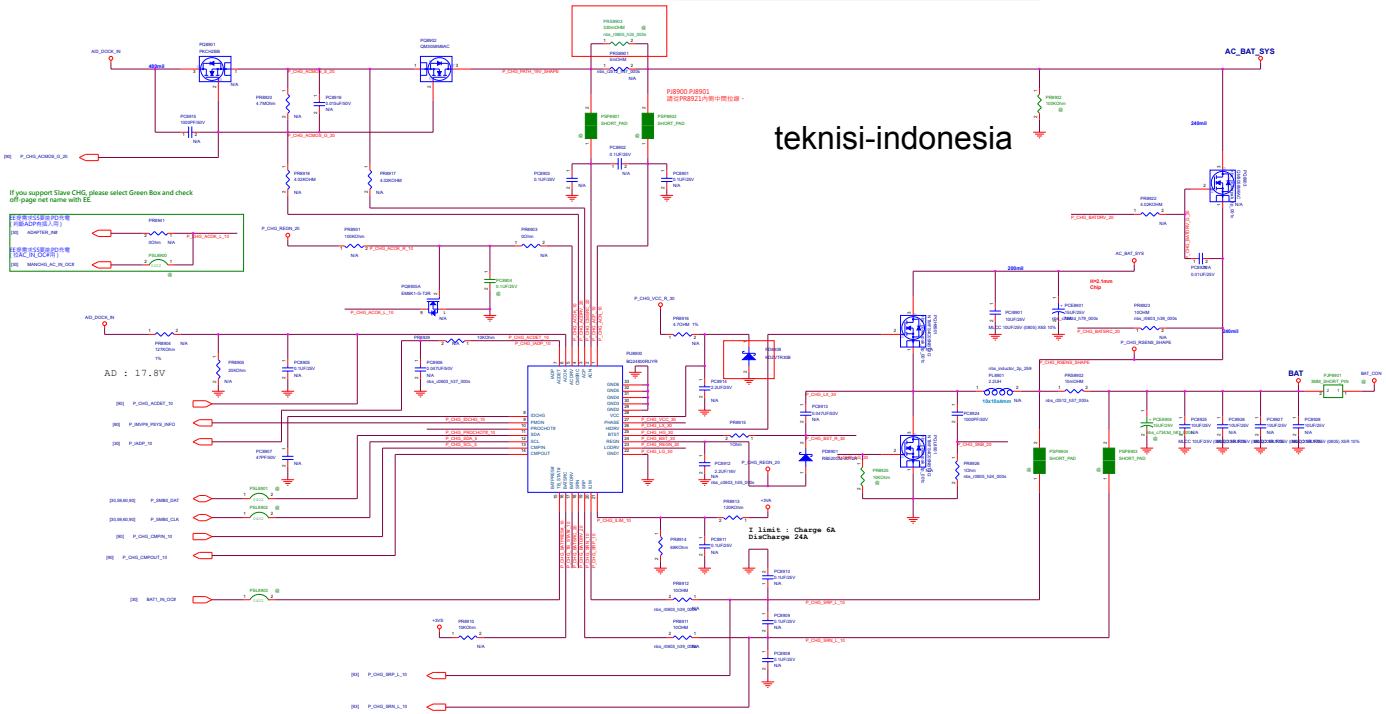


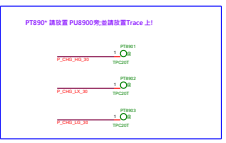
<Variant Name>

Project Name: Project Name		Rev: R1.0
Title : PW_+12VS_FAN		
Size: A4	Dept.: NB Power team	Engineer: Power RD
Date: Wednesday, March 17, 2021	Sheet 96 of 103	

Main Board

PRS8901	ADP<120W	ADP<=200W	ADP>200W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0038S103	10108-0008B000	10108-0008B000





HW_Throttle

AC limit = 100% ADP
Bat limit = byte 7 x 1.7

dGPU_PD# ---> GPIO12(EE page 75 or 78)

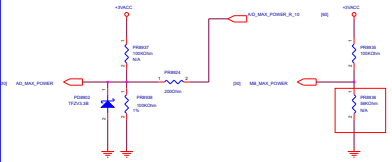
Plug HW Throttle(Out)

Plug HW Throttle(In)

AD : 17.5V
Place Close to PD8901

POP window

Adaptor select
total power = 90% ADP



Adaptor select

	N Series	N Series
PRS8901	10m	5m
PR8936		
14K 10021215001A030	0.4V	45W 120W
31.6K 10021215401A030	0.8V	150W 150W
56K 10021215601A030	1.2V	180W 180W
93.1K 10021215931A030	1.6V	65W 230W
150K 10021216501A030	2.0V	NA 280W
270K 10021217201A030	2.4V	90W 200W
560K 10021218101A030	2.8V	120W 240W

Project Name	Coffee lake-H
Title :	PW_CHARGER
Dept.:	NB Power Team
Engineer:	Benson
Date:	Wednesday, March 17, 2021

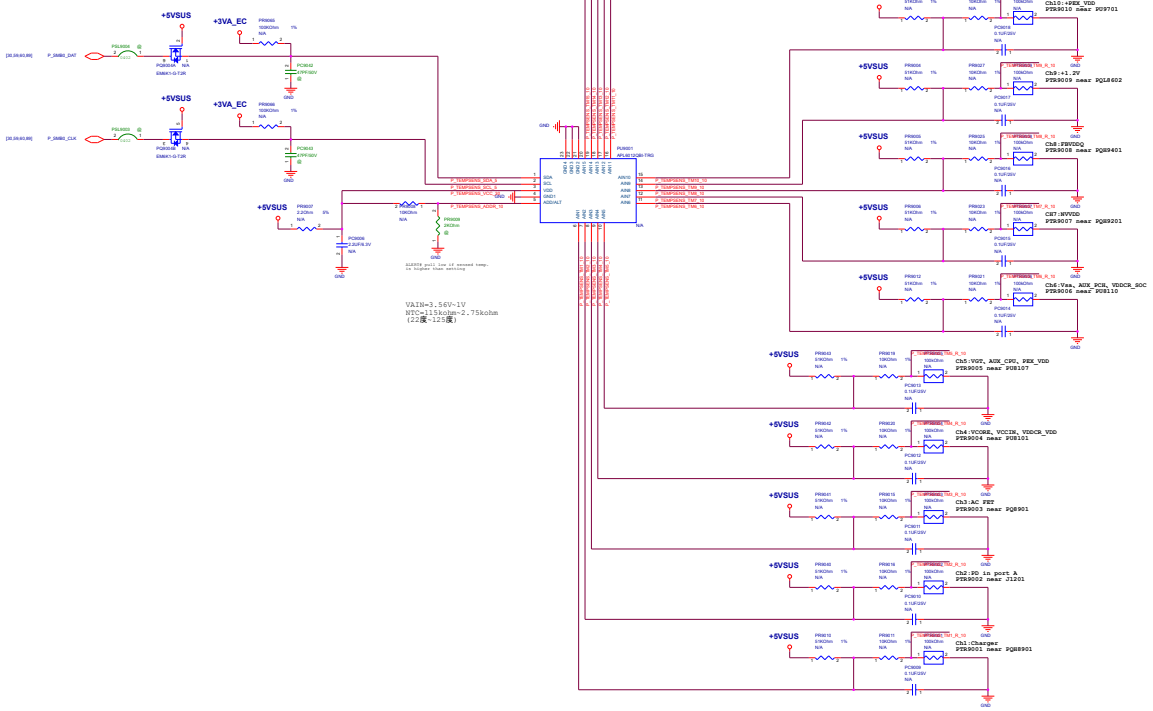
P90_PROTECTION

Address Selection Table

Address	0x78	0x79	0x7A	0x7B	0x7C	0x7D	0x7E	0x7F
PU9031	10k	1.5k	2k	3.4k	4.9k	6.8k	8.2k	9k
PU9032	Open	8.2k	6.2k	4.8k	3.7k	2.8k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function		Temp. alert threshold setting		Sensed temp. data			bit 6 = 0 bit 5 = 0 bit 4 = 0 Over 125°C detect

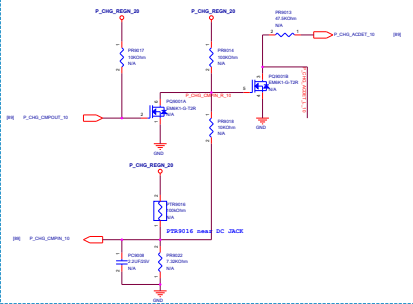


NTC	CML	TGL
CH15	PD in port B	PD in port B
CH14	Slave Charger	Slave Charger
CH13	1.8VSUS	1.8VSUS
CH12	5VSUS	5VSUS
CH11	3VA_DSW	3VA_DSW
CH10	1.05VSUS	PEX_VDD
CH09	1.2V	1.2V
CH08	FBVDDQ	FBVDDQ
CH07	NVVDD	NVVDD
CH06	Vas	AUX_PCH
CH05	VGT	AUX_CPU
CH04	VCORE	VCCIN
CH03	AC FET	AC FET
CH02	PD in port A	PD in port A
CH01	Charger Mos	Charger Mos

NTC	AMD
CH15	PD in port B
CH14	Slave Charger
CH13	1.8VSUS
CH12	5VSUS
CH11	3VA_DSW
CH10	0.75VSUS
CH09	1.2V
CH08	FBVDDQ
CH07	NVVDD
CH06	VDDCR_SOC
CH05	PEX_VDD
CH04	VDDCR_VDD
CH03	AC FET
CH02	PD in port A
CH01	Charger Mos

OVP Protection circuit 24V==>Cost down

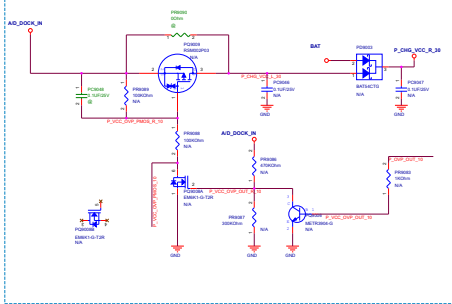
DC JACK_Protection



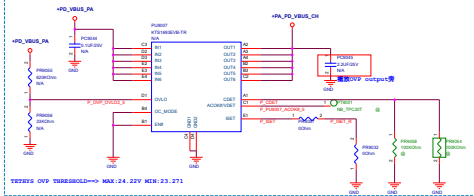
AC_Short_Protection

GPU over power

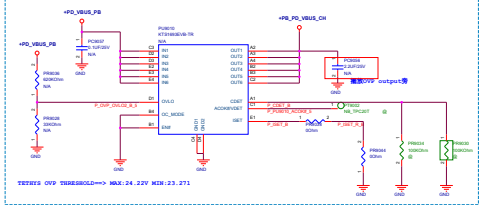
VCC pin OVP Protection circuit 24V



OVP for type C input (Slave Charger)

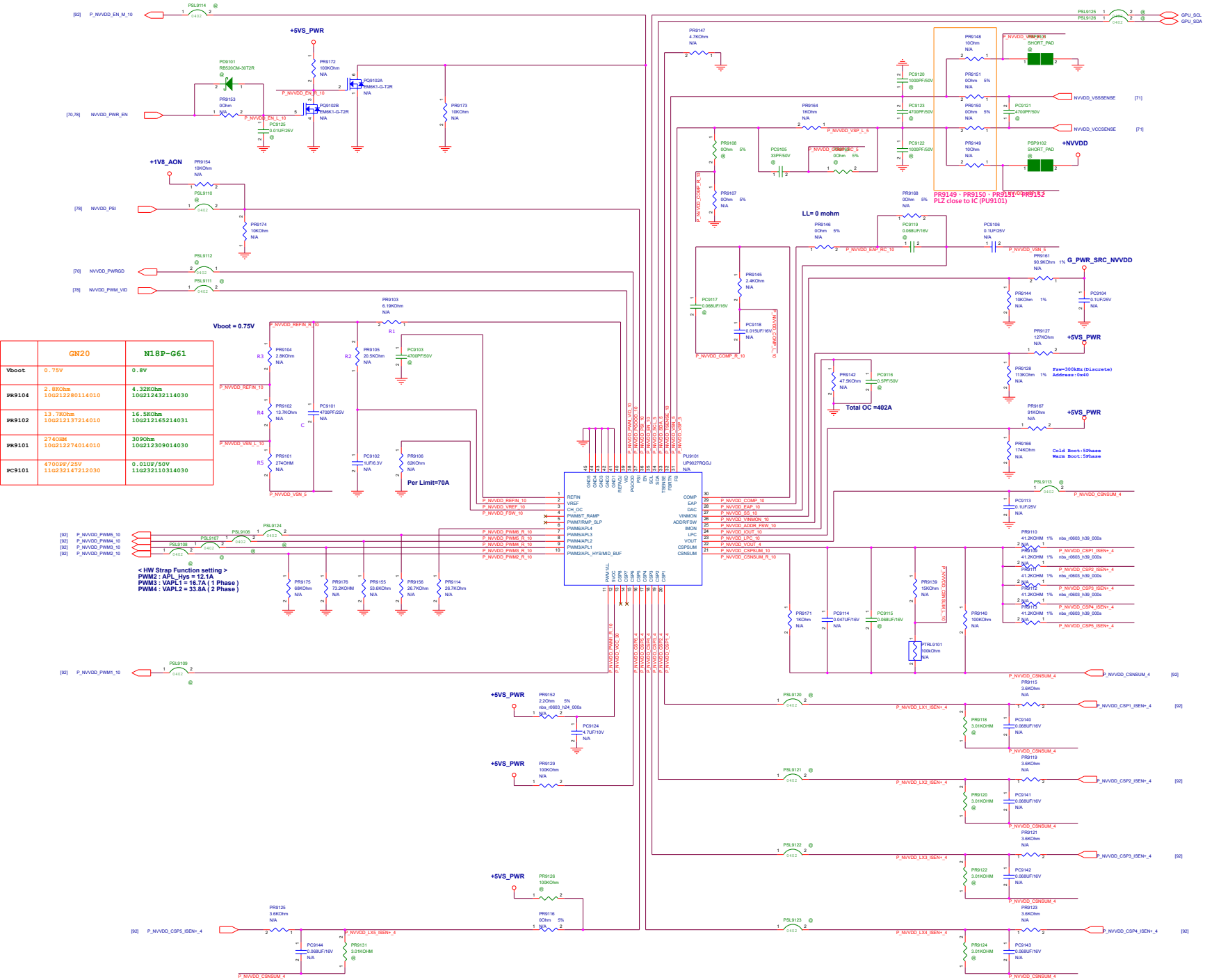


OVP for type C input 2 (Add for second PD port)



<Variant Name>
ASUS Project
Title : PW_PROTECTION
Size: A3
Dept.: MB Power Team
Engineer: Power RD
Date: Wednesday, March 17, 2021
Sheet: 90 of 103

+NVVDD [For DGPU] UP9027R_Dual_11*6_5Ph

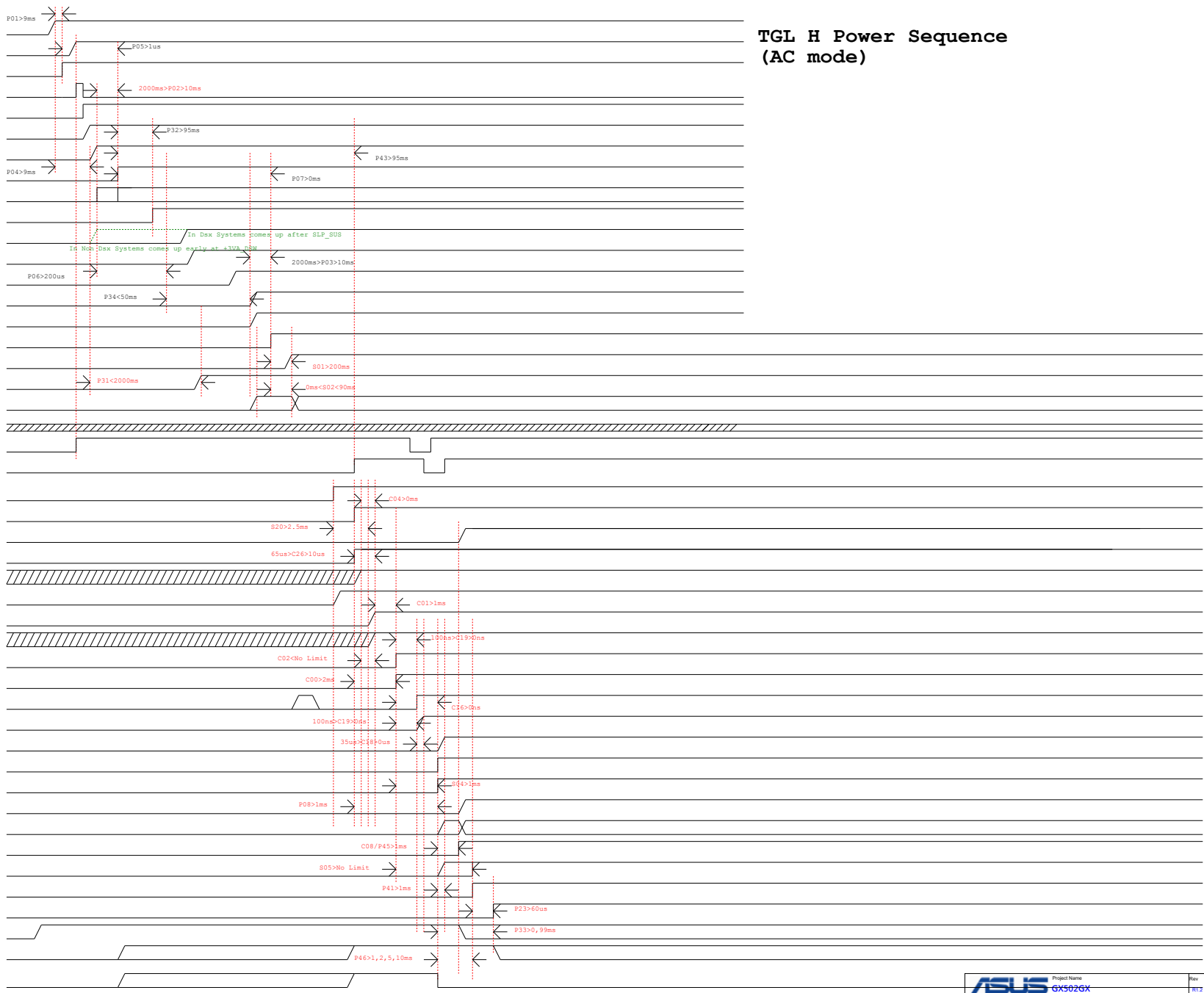


	GN20	N18P-G61
Vboot	0.75V	0.8V
PR9104	2.8KOhm 10G212280114010	4.32KOhm 10G2124321140 30
PR9102	13.7KOhm 10G212137 1401 0	16.5KOhm 10G212165214031
PR9101	274OHM 10G212274014010	309Ohm 10G212309014030
PC9101	4700PF/25V 11G232147212030	0.01UF/50V 11G232110314030

AC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

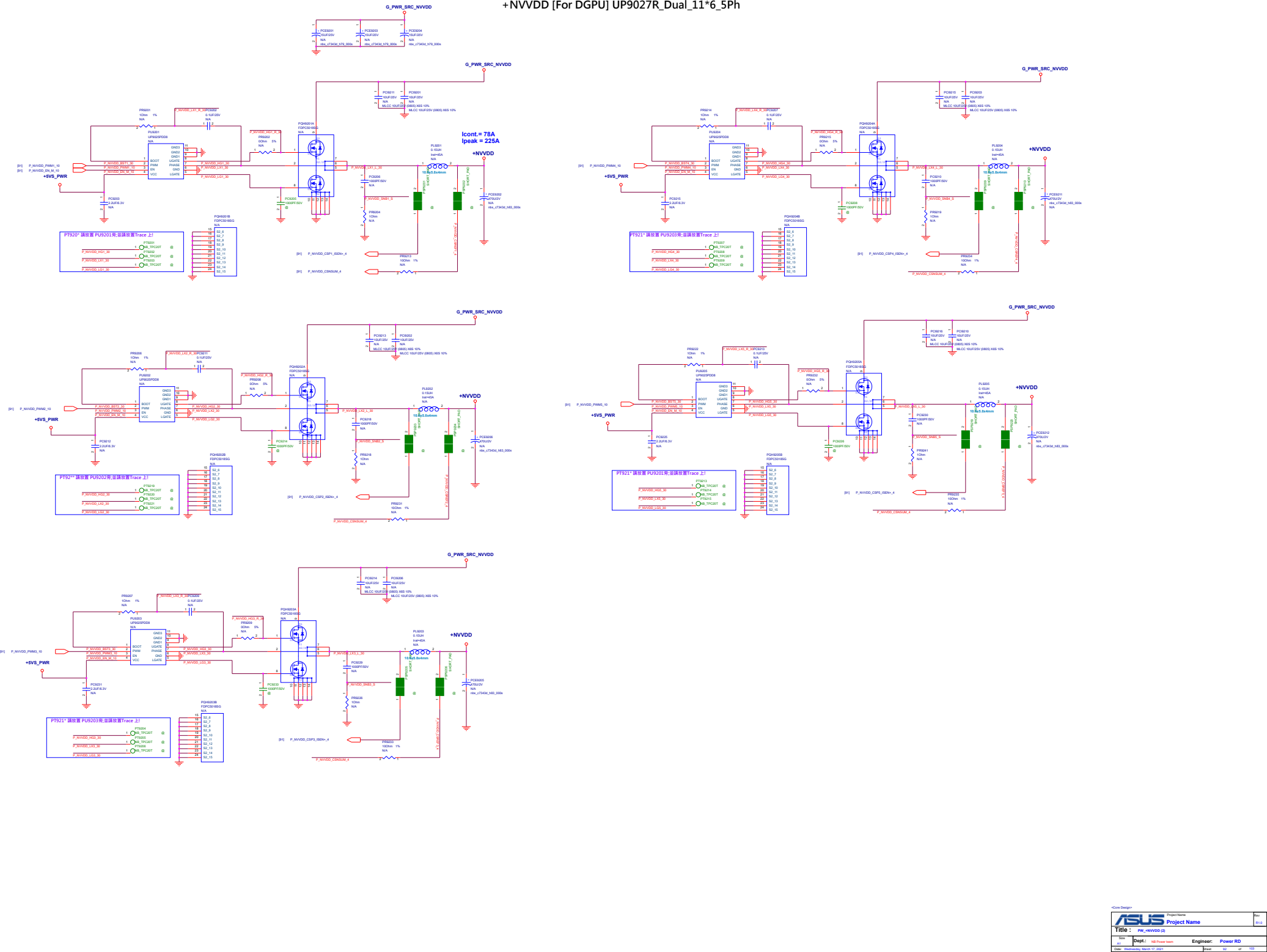
(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +3VSUS (P_3VSUS_PWRGD)
(VSUS_ON) +1.8VSUS (1.8VSUS_PWRGD)
+VCC1.05_OUT_FET
+VCC_VNNEXT_1P05
+VCC_V1P05EXT_1P05
(EC) PM_RSMRST#_X1 (PCH)
(PCH) ME_SusPwrDnAck (EC)
(PCH) SUS_CLK
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(PCH) PM_SUSC# (EC)
(PCH) PM_SUSB# (EC)
(SUSB_EC#) +12VS/+5VS/+3VS
(PCH) CPU_C10_GATE# (CPU)
(SUSC_EC#) +1.05V_VCCST
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +1.2V (1.2V_PWRGD)
(+VCC1.05_OUT_FET) +VCCSTG
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(CPU) DDR_PG_CTRL (Power)
(1.2V_ON) +VTT (1.2V_PWRGD)
VCCIN
IMVP9_PWRGD
(EC) PM_PWROK_X1 (PCH)
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(PCH) CLK_PCI_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(EC) PM_SYSPWROK_X1 (PCH)
(PCH) PCH_SUS_STAT#
(PCH) BUF_PLT_RST# (EC)
(CPU) PCH_THERMTRIP# (PCH)
(CPU) P_SVID_DATA_500HM_X2 (Power)
(CPU) P_SVID_ALERT#_50OHM_X2 (Power)



TGL H Power Sequence (AC mode)

ASUS	Project Name: GX502GX		Rev: R1.2
Title : Power On Timing-AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Wednesday, March 17, 2021	Sheet 100 of 103		

+NVVDD [For DGPU] UP9027R_Dual_11*6_5Ph

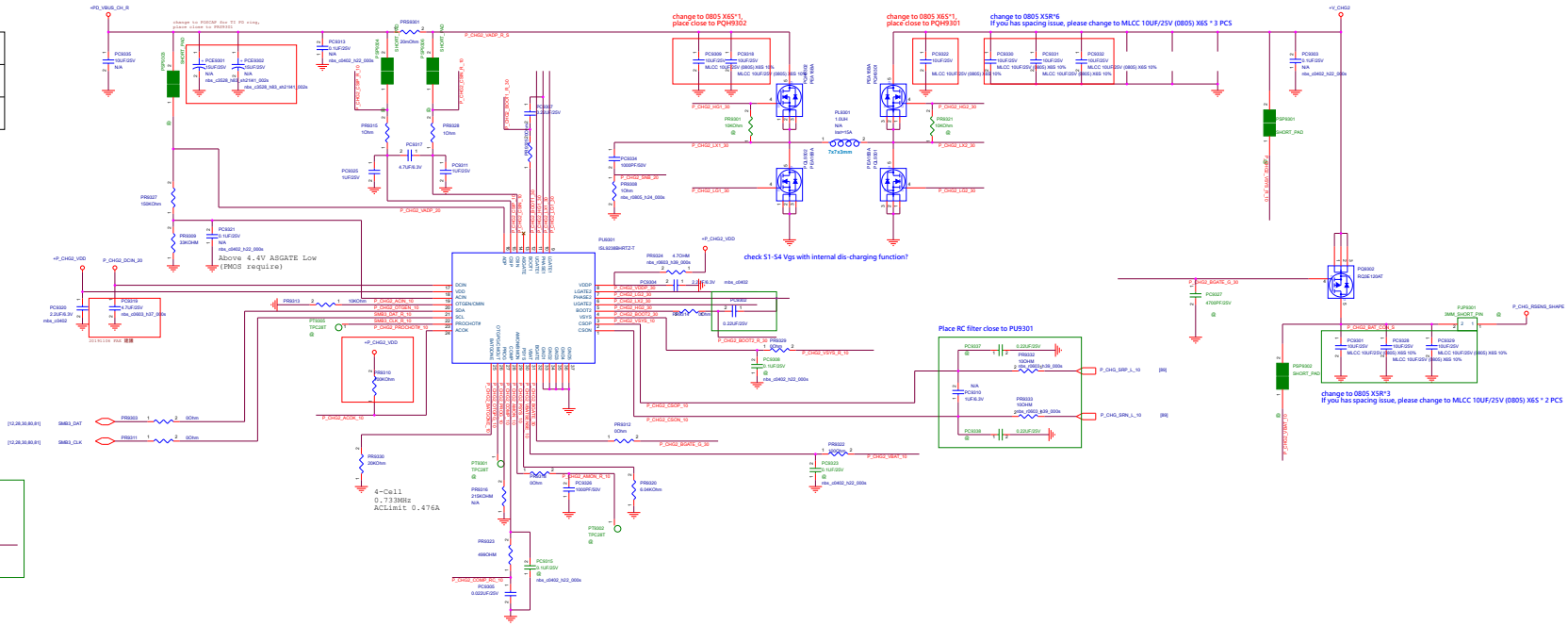


<Core Design>

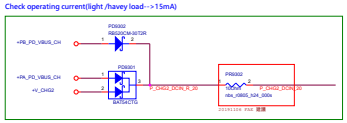
ASUS	Project Name: Project Name		Rev: R1.0
Title : PW_+NVVDD (2)			
Size: A1	Dept.: NB Power team	Engineer: Power RD	
Date: Wednesday, March 17, 2021	Sheet: 92 of 103		

Charger ISL9238 (NVDC)

	65W	100W
PL9301	INDUCTOR 1.0UH/11A 20% 09016-00012800	INDUCTOR 1.0UH/15A 20% 09016-00012600
PCE9302	@	N/A

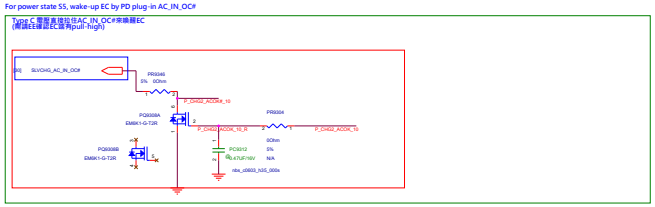


Check operating current(light /havey load-->15mA)



For power state S5, wake-up EC by PD plug-in AC_IN_OC#

Table C 電源表現功能AC_IN_OC#常態顯EC
(常態EC輸出High)



Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER INC.

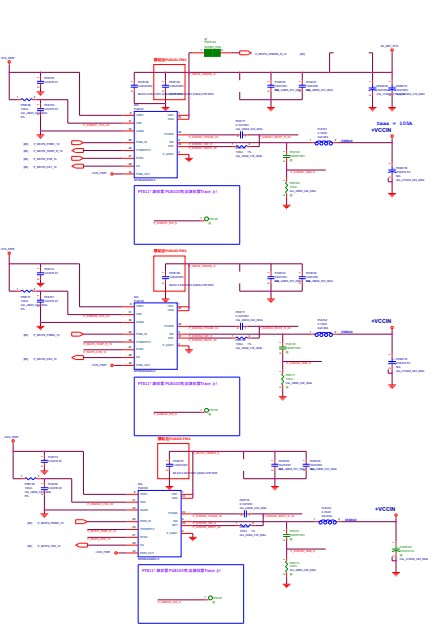
Title : Revision History

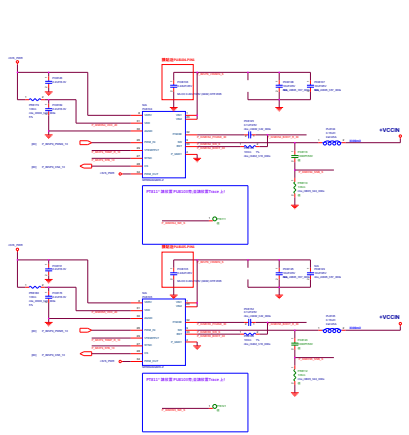
Engineer: EE

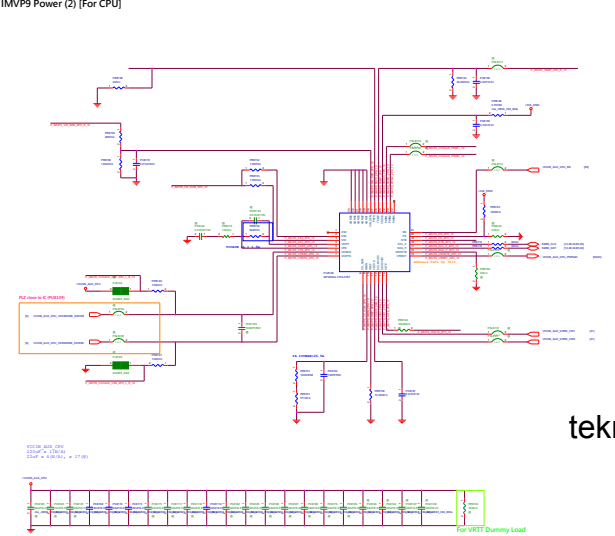
Size: D | Project Name: GX502GX | Rev: R1.2

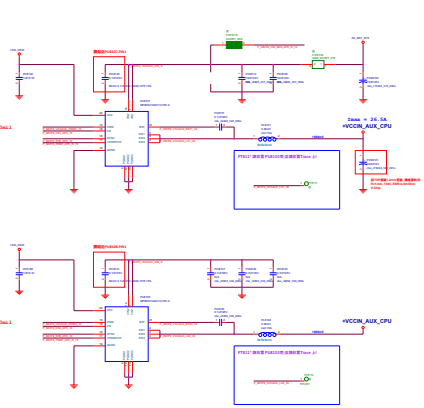
Date: Wednesday, March 27, 2019 | Sheet 102 of 105

Tiger Lake-H IMVP9 Power (2) [For CPU]









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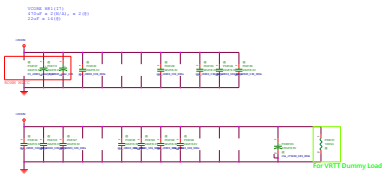
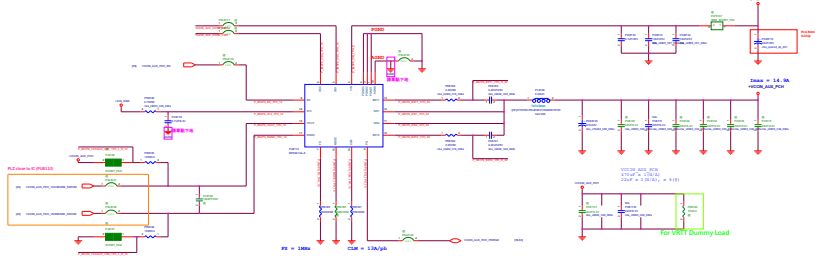




EE PART

GX502GX R1.1 SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							

ASUSTeK COMPUTER		Title :	GX502GX_SKU Table_R1.0
		Engineer:	EE
Size	Project Name		Rev
B	GX502GX		R1.1
Date: Wednesday, March 17, 2021		Sheet 103 of 105	

13. Audio Codec : 02043-00130000 (663-VA4)

<Core Design>

Title : OTH_for test only

ASUSTeK COMPUTER

Engineer: EE

Size	Project Name	Rev
A	GX502GX	R1.2

Date:	Wednesday, March 17, 2021	Sheet	95	of	103

PEX_VDD [For GPU]

	GN20	N18P-G61
Vo	0.95V	1V

Imax= 4.42A
OCP=8A
+PEX_VDD

AC_BAT_SYS
PJP9702
1MM_SHORT_PIN
@

PCI9703
10UF/25V
@
MLCC 10UF/25V (0805) X6S 10%

PCI9704
10UF/25V
N/A
MLCC 10UF/25V (0805) X6S 10%

PU9702
HPA02240RVER
N/A

P_PEX_VDD_VIN_S
P_PEX_VDD_5V_10
P_PEX_VDD_OC_10
P_PEX_VDD_SLEW_10
P_PEX_VDD_VSENS_10

VIN1 VIN2 VIN3 V5 GND TRIP SLEW VSNS GSNS
SW4 SW3 SW2 SW1 BST NC MODE LP# PGOOD
REFIN2 REFIN VREF NU EN GND1 GND2 GND3 GND4 GND5
PGND5 PGND4 PGND3 PGND2 PGND1

P_PEX_VDD_LX_30
P_PEX_VDD_BST_30
P_PEX_VDD_PG_10

PC9710
0.1UF/25V
N/A

PR9707
0Ohm
N/A

PL9702
1UH
N/A
Irat=11A
5x5x3mm

PSP9702
SHORT_PAD
[70]

PSL9702
P_PEX_VDD_BST_R_30
0402
@
PEXVDD_PWRGD

PC9715
22UF/6.3V
N/A

PCE9701
330UF/2.5V
N/A
hbs_c3528_h83_sh21l41_002s

PC9711
3300PF/50V
N/A

+5VSUS
PR9709
4.7OHM 5%
N/A

PC9706
4.7UF/6.3V
N/A

+5VSUS
PR9703
0Ohm
@

PR9704
0Ohm
N/A

P_PEX_VDD_REFIN_10
P_PEX_VDD_VREF_10
P_PEX_VDD_EN_10

PR9705
39KOhm
N/A

PR9706
36KOhm
N/A

PC9708
0.22UF/25V
N/A

P_PEX_VDD_LOSENS_10

PR9710
10Ohm
N/A
P_PEX_VDD_VSENS_10

PR9711
0Ohm
N/A
PS_PEXDVDD_FB_R [70]

PD9703
RB520CM-30T2R
@

PR9708
0Ohm
N/A
[70] PEXVDD_PWR_EN

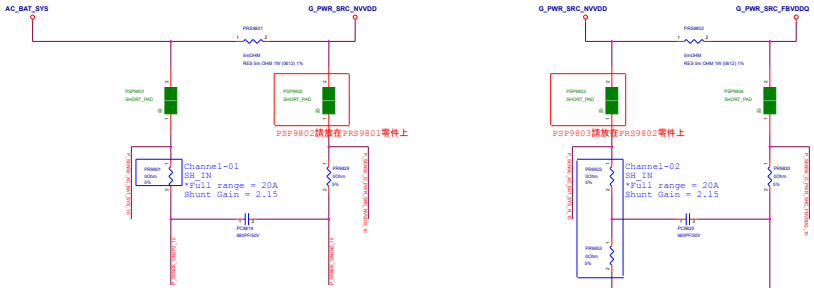
P_PEX_VDD_EN_10
PC9712
0.1UF/25V
@

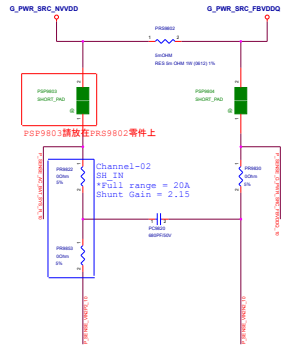
PT840* 請放置 PU8401旁;並請放置Trace 上!
PT9701
@
P_PEX_VDD_LX_30
TPC20T

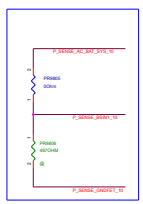
	GN20	N18P-G61
PR9705	39KOhm 10G212390214030	36KOhm 10G212360214030
PR9710	10Ohm 10G21210R014010	0Ohm 10G212000004030
PR9711	0Ohm 10G212000004030	@

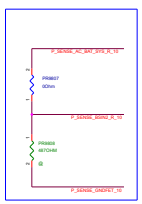
ASUS	Project Name: G703GI	Rev: R1.0
Title : *****		
Size: A4	Dept.: ASUSTeK COMPUTER INC. Engineer: Power RD	
Date: Wednesday, March 17, 2021	Sheet 97 of 103	

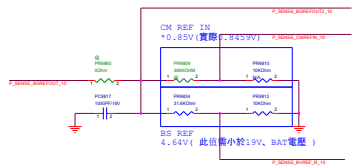
	PR9801	PR9822	PR9853
GN20	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
N18P-G61	100Ohm 10G212100014010	49.9Ohm 10G212491R914010	49.9Ohm 10G212491R914010



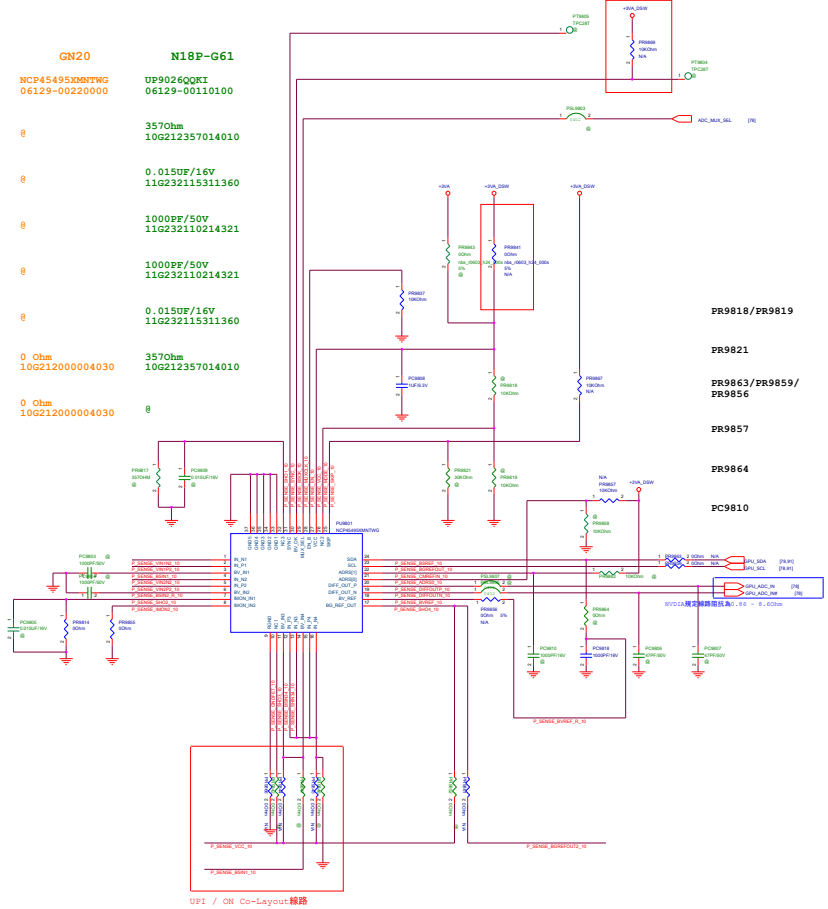


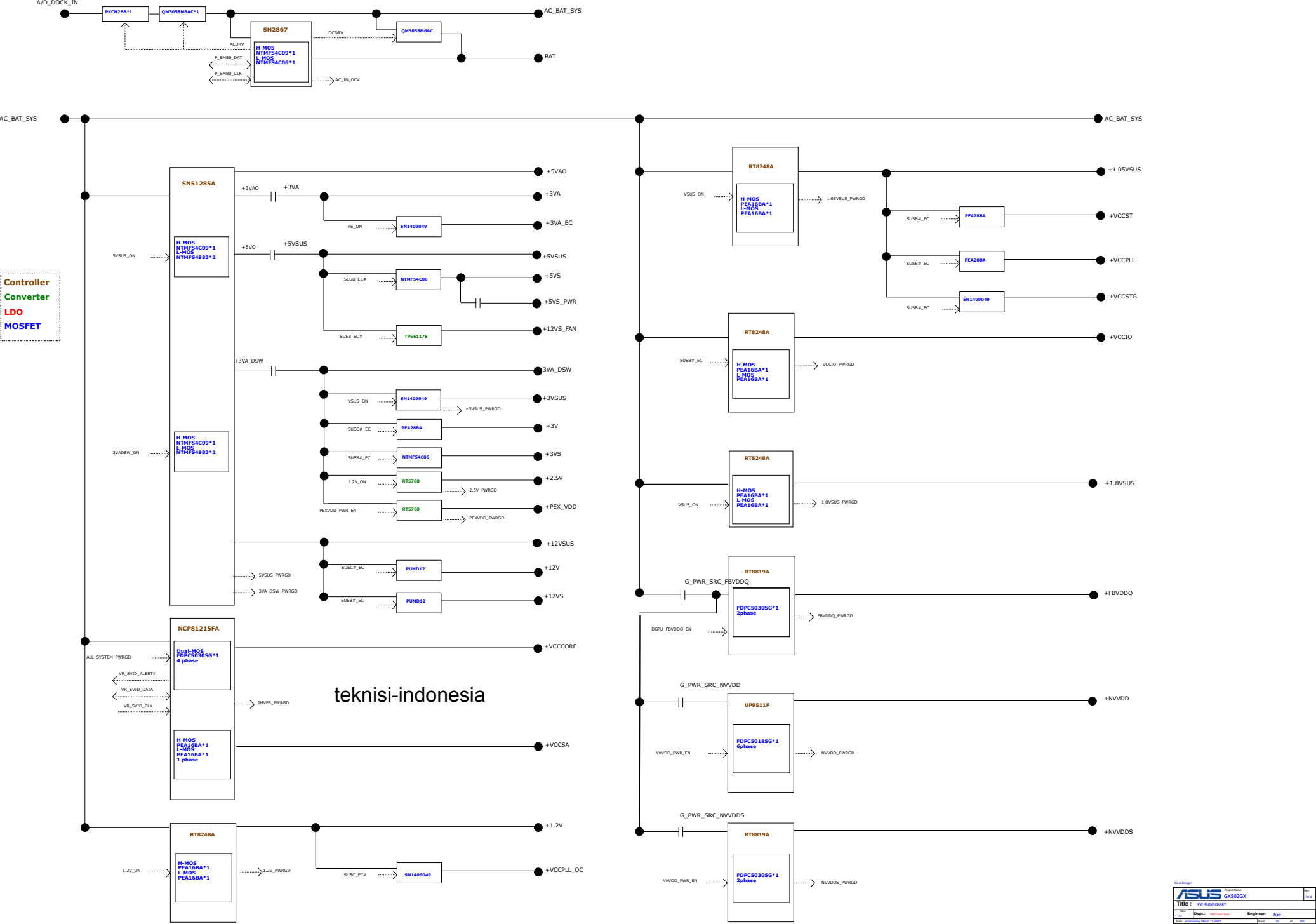






	GN20	N18P-G61
PU9801	NCP45495XMNTWG 06129-00220000	UP9026QQKI 06129-00110100
PR9817	@	357Ohm 10G212357014010
PC9809	@	0.015UF/16V 11G232115311360
PC9803	@	1000PF/50V 11G232110214321
PC9804	@	1000PF/50V 11G232110214321
PC9805	@	0.015UF/16V 11G232115311360
PR9814	0 Ohm 10G212000004030	357Ohm 10G212357014010
PR9855	0 Ohm 10G212000004030	@




A/D_DOCK_IN
PKCH2BB*1
QM30S8M6AC*1
SN2867
H-MOS NTMFS4C09*1 L-MOS NTMFS4C06*1
ACDRV
DCDRV
P_SMB0_DAT
P_SMB0_CLK
AC_IN_OC#
QM30S8M6AC
AC_BAT_SYS
BAT
Controller
Converter
LDO
MOSFET
SN51285A
+3VAO
+3VA
+5VO
+5VSUS
3VADSW_ON
5VSUS_ON
PS_ON
SUSB_EC#
SUSC#_EC
SUSB#_EC
VSUS_ON
1.2V_ON
PEXVDD_PWR_EN
5VSUS_PWRGD
3VA_DSW_PWRGD
+3VA_DSW
+5VAO
+3VA_EC
+5VSUS
+5VS
+5VS_PWR
+12VS_FAN
3VA_DSW
+3VSUS
+3V
+3VS
+2.5V
+PEX_VDD
+12VSUS
+12V
+12VS
SN1409049
NTMFS4C06
TPS61178
PEA288A
RT5768
PUMD12
+3VSUS_PWRGD
2.5V_PWRGD
PEXVDD_PWRGD
NCP81215FA
Dual-MOS FDPC5030SG*1 4 phase
H-MOS PEA168A*1 L-MOS PEA168A*1 1 phase
ALL_SYSTEM_PWRGD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
IMVP8_PWRGD
+VCCCORE
+VCCSA
RT8248A
H-MOS PEA168A*1 L-MOS PEA168A*1
1.2V_PWRGD
SUSC_EC#
+1.2V
+VCCPLL_OC
RT8248A
H-MOS PEA168A*1 L-MOS PEA168A*1
VSUS_ON
1.05VSUS_PWRGD
+1.05VSUS
+VCCST
+VCCPLL
+VCCSTG
SUSB#_EC
RT8248A
H-MOS PEA168A*1 L-MOS PEA168A*1
VCCIO_PWRGD
+VCCIO
RT8248A
H-MOS PEA168A*1 L-MOS PEA168A*1
VSUS_ON
1.8VSUS_PWRGD
+1.8VSUS
RT8819A
FDPC5030SG*1 2phase
G_PWR_SRC_FBVDDQ
DGPU_FBVDDQ_EN
FBVDDQ_PWRGD
+FBVDDQ
G_PWR_SRC_NVVDD
UP9511P
FDPC5018SG*1 6phase
NVVDD_PWR_EN
NVVDD_PWRGD
+NVVDD
G_PWR_SRC_NVVDDS
RT8819A
FDPC5030SG*1 2phase
NVVDD_PWR_EN
NVVDDS_PWRGD
+NVVDDS
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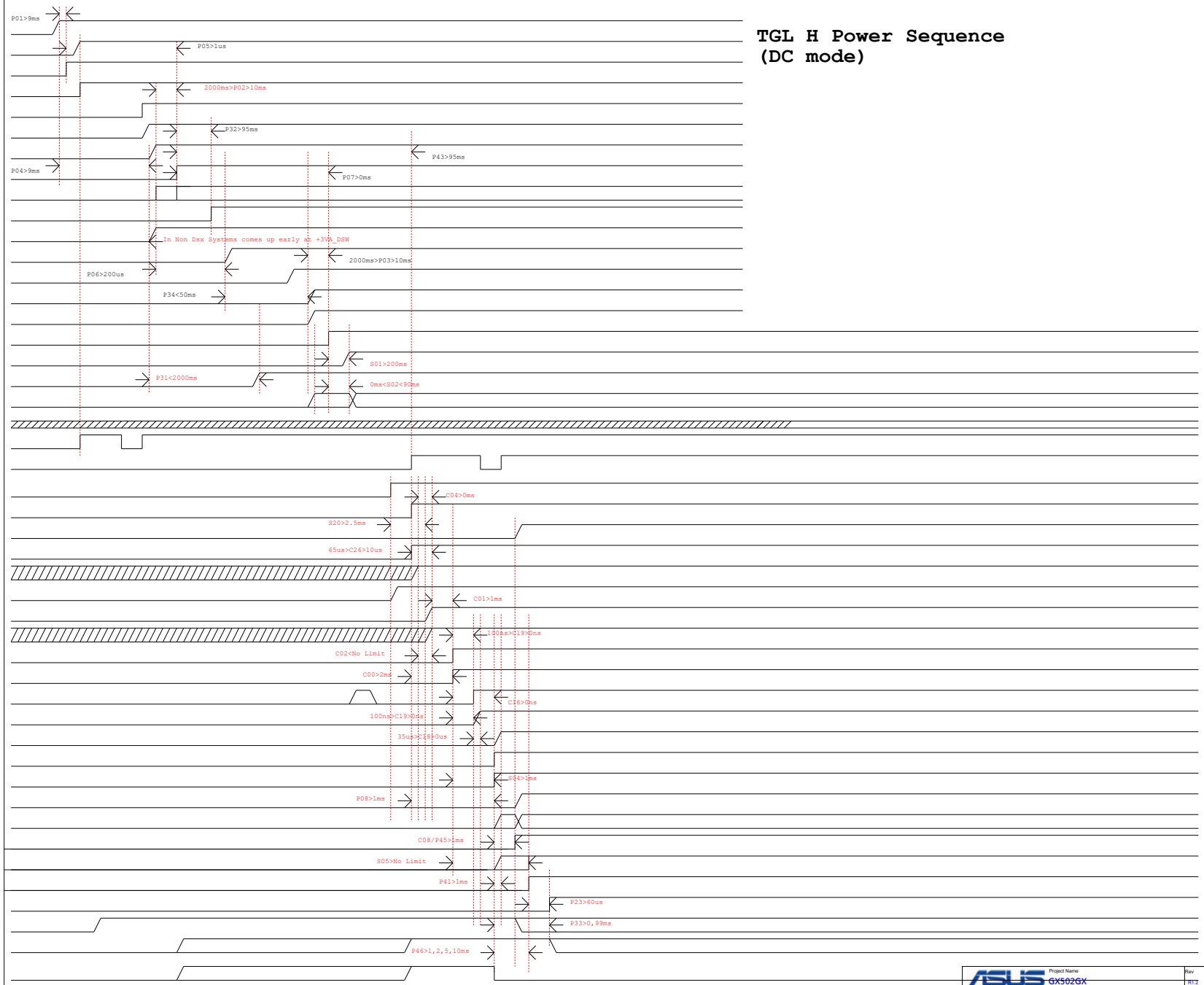
ASUS
Project Name GX502GX
Title : PW_FLOW CHART
Dept.: NB Power team
Engineer: Joe
Date: Wednesday, March 17, 2021

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +3VSUS (P_3VSUS_PWRGD)
(VSUS_ON) +1.8VSUS (1.8VSUS_PWRGD)
+VCC1.05_OUT_FET
+VCC_VNNEXT_1P05
+VCC_V1P05EXT_1P05
(EC) PM_RSMRST#_X1 (PCH)
(PCH) ME_SusPwrDnAck (EC)
(PCH) SUS_CLK
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(PCH) PM_SUSC# (EC)
(PCH) PM_SUSB# (EC)
(SUSB_EC#) +12VS/+5VS/+3VS
(PCH) CPU_C10_GATE# (CPU)
(SUSC_EC#) +1.05V_VCCST
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +1.2V (1.2V_PWRGD)
(+VCC1.05_OUT_FET) +VCCSTG
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(CPU) DDR_PG_CTRL (Power)
(1.2V_ON) +VTT (1.2V_PWRGD)
VCCIN
IMVP9_PWRGD
(EC) PM_PWROK_X1 (PCH)
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(PCH) CLK_PCI_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(EC) PM_SYSPWROK_X1 (PCH)
(PCH) PCH_SUS_STAT#
(PCH) BUF_PLT_RST# (EC)
(CPU) PCH_THERMTRIP# (PCH)
(CPU) P_SVID_DATA_50OHM_X2 (Power)
(CPU) P_SVID_ALERT#_50OHM_X2 (Power)



TGL H Power Sequence (DC mode)

ASUS	Project Name: GX502GX		Rev: R1.2
Title : Power On Timing--DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Wednesday, March 17, 2021	Sheet 101 of 103		